Investigation of Electrical Component Failures Affecting Vehicle Electronics

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Clemson University

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INVESTIGATION OF ELECTRICAL COMPONENT FAILURES AFFECTING VEHICLE ELECTRONICS

A Dissertation
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
Automotive Engineering

by
Dexin Zhang
December 2014

Accepted by:
Dr. Todd H. Hubing, Committee Chair
Dr. Pierluigi Pisu
Dr. Robert Prucka
Dr. Simona Onori
ABSTRACT

This dissertation describes three independent studies related to electrical component failures affecting vehicle electronics. The topics covered are: comparison of the accelerator-pedal-to-engine-control module (AP-to-ECM), the effect of electrical fast transients on multi-layer ceramic (MLC) capacitors, and electrical behavior of MLC capacitors damaged by electrostatic discharge.

The first chapter examines the AP-to-ECM interfaces of five vehicles equipped with electronic throttle control systems. All five vehicles employ simple voltage level sensing from two or three sensors in the accelerator pedal assembly. The purpose of the study is to identify any differences in the AP-to-ECM interfaces of vehicles with high reported rates of unintended acceleration compared to vehicles with low reported rates of unintended acceleration. The study does not attempt to identify the root causes of unintended acceleration; however it points out important design issues that suggest a set of best practices for electronic throttle control design.

The second chapter investigates the susceptibility of MLC capacitors to high-voltage electrical fast transients (EFTs). X7R and NP0 MLC capacitors with a 50-V voltage rating and 0603 package size were tested. X7R capacitors often failed during a spike in the voltage, but exhibited no obvious degradation in the measured insulation resistance at low voltages immediately after the failure. NP0 capacitors usually failed by suddenly shorting and maintaining the short after the failure. With the application of additional voltage spikes, some X7R capacitors exhibited a full recovery in terms of the measured resistance, returning to their initial state. The resistance of an X7R capacitor damaged by an EFT event
is a function of the applied voltage. The terminal impedance can be modeled as two diodes in parallel.

The third chapter investigates the electrical behavior of MLC capacitors subjected to electrostatic discharge (ESD). The degradation of MLC capacitors subjected to repeated discharges manifests itself as a non-linear resistance. The leakage current in degraded capacitors increases exponentially with an applied voltage. The I-V characteristics of these capacitors are symmetric with voltage and independent of the polarity of the ESD discharges responsible for the degradation. A model for a degraded capacitor consisting of two parallel diodes with opposite polarities is proposed.
ACKNOWLEDGEMENTS

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CHAPTER ONE

COMPARISON OF THE AP-TO-ECM INTERFACES ON VEHICLES WITH LOW AND HIGH REPORTED RATES OF UNINTENDED ACCELERATION

Dexin Zhang and Todd H. Hubing

Abstract

This paper examines the AP-to-ECM interfaces of five vehicles equipped with electronic throttle control systems. All five vehicles employ simple voltage level sensing from two or three sensors in the accelerator pedal assembly. The purpose of the study is to identify any differences in the AP-to-ECM interfaces of vehicles with high reported rates of unintended acceleration compared to vehicles with low reported rates of unintended acceleration. The study does not attempt to identify the root causes of unintended acceleration; however it points out important design issues that suggest a set of best practices for electronic throttle control design.

I. INTRODUCTION

A. Problem Statement

It has been proposed that an increase in reports of sudden unintended acceleration in recent years might be the result of problems with the design of the electronic systems. Electronic throttle control (ETC) systems have been the subject of particular scrutiny. In the U.S., the National Highway Traffic Safety Administration (NHTSA) keeps a database of consumer complaints related to vehicle safety [1]. As noted in a recent NASA investigation of unintended acceleration in Toyota vehicles, several models experienced
sharp increases in the number of complaints related to unintended acceleration in model years corresponding to the introduction of new or modified electronic throttle control systems [2].

B. Research Background

Electronic throttle control systems began appearing in vehicles 10 - 15 years ago, replacing the throttle cable that made a direct mechanical connection between the accelerator pedal (AP) and the engine throttle. In vehicles with electronic throttle control, the engine control module (ECM) senses the position of the accelerator pedal electronically and uses that information to determine what the throttle opening should be.

Ten years ago, most electronic throttle control systems employed two or three sensors in the accelerator pedal assembly. These sensors were typically potentiometers (or later Hall-effect sensors) that were powered by a 5-volt supply in the ECM. They returned a voltage to the ECM that varied depending on the amount that the accelerator pedal was depressed. If the pedal positions indicated by any two sensors were inconsistent, the ECM was designed to recognize a potential problem and take an appropriate action to keep the vehicle occupants safe.

The use of multiple sensors certainly improved the safety of these early electronic throttle control systems; however these systems were not foolproof. Typically, the technology used by the redundant sensors was the same, making them vulnerable to the same types of failures. To be truly redundant, these sensors should have employed electrically isolated voltage references to prevent a single point electrical short/open condition from invalidating all sensor outputs [3]; however this was not always the case.
In many of these systems, it was possible for a bad voltage reference or two bad sensor outputs to emulate a depressed accelerator pedal.

Since electrical faults can emulate valid pedal voltages in the AP-to-ECM interfaces described above, many automotive manufacturers currently employ interfaces with encoded signals. For example, [4] describes an interface used by at least one manufacturer where one of the accelerator pedal position (APP) signals is grounded periodically by a circuit in the ECM in order to detect a possible short circuit between the two APP signals. With the introduction of Hall-effect and other non-contact sensors in accelerator pedal assemblies, it has become more practical to employ digital communications in the AP-to-ECM interface [5]. On several Volvo models [6, 7] and the 2011 Ford Fiesta [8], one of the pedal sensors generates a pulse-width-modulated signal and the other a simple voltage level.

Despite these technology advances, a large number of vehicle makes and models still employ accelerator pedal position sensors with simple analog voltage outputs. Some of these vehicles have historically had relatively high rates of reported unintended acceleration, while others have had very few reported problems. This paper examines the AP-to-ECM interfaces of five vehicles equipped with electronic throttle control systems employing analog voltage pedal interfaces. The purpose of this study is to identify differences in the AP-to-ECM interfaces of vehicles with high reported rates of unintended acceleration compared to vehicles with low reported rates on unintended acceleration.
C. Research Approach

The vehicles selected for this study are listed in Table 1.1. They are ranked according to the rate of consumer complaints related to unintended acceleration as registered in the NHTSA complaint database as of September 29, 2014. The database was parsed by vehicle make, model and model year. Only complaints categorized in the database as “Vehicle Speed Control” were examined. Furthermore, only complaints that specified an unintended acceleration or unintended throttle opening were included. Complaints related to unintentional deceleration or speedometer failures without an accompanying acceleration were not counted. Also, complaints that clearly specified the cause of the acceleration as being due to cruise control failures or pedal misapplication were not counted.

Vehicles deemed to have relatively high rates of reported UA were the 2005 Toyota Camry, the 2005 Ford Mustang and the 2006 Ford Explorer. Vehicles with relatively low rates of reported UA were the 2001 Volkswagen Jetta and the 2008 GMC Sierra. The following sections describe the AP-to-ECM interfaces for each of these vehicles with a
particular emphasis on differences that may affect the likelihood of experiencing unintended acceleration.

D. **Broad Impact**

A number of 9698 VOQ reports from the NHTSA database received from 2000 to 2010 were identified as UA events based on experts reviews and analysis [2]. This means, in average, there were almost three UA events each day during this period in US. Many of them have caused injuries and fatalities to the drivers and passengers which results in a great concern not only to the public but also to the automotive industry. Of many various factors accounting for UA events, failures of electronic control systems affecting the throttle control function have been raising concerns continuously. The AP-to-ECM interface of the ETC system is particularly under focus since its failure detection could only rely on the interface itself (open-loop) and the failure could be misinterpreted as drivers’ inputs.

This research proposes focus on the comparison of the AP-to-ECM interfaces on vehicles with low and high reported rates of unintended acceleration. The study identifies differences in the AP-to-ECM interfaces of vehicles with high reported rates of unintended acceleration compared to vehicles with low reported rates of unintended acceleration. Based on the findings in this study, important design issues that suggest a set of best practices for electronic throttle control design are pointed out to help automotive system manufacturers to enhance their products’ immunities to various failures. The study does not attempt to identify the root causes of UA; however it will be demonstrated in the following two chapters that a filtering capacitor in an automotive application such as the
AP-to-ECM interface could been failed to cause shifts of the signal voltages in electrically noisy environments. The shifts of DC voltage levels could been regarded as valid inputs with the AP-to-ECM interface.

II. THE AP-TO-ECM DIAGNOSTIC INTERFACE

For the 2005 Camry, the 2008 Sierra and the 2001 Jetta, depressing the accelerator actuates two separate potentiometers that provide a variable resistance to two separate inputs of the ECM. Although the two sensors are nominally independent, they use the same technology and reside in the same package. They provide input voltages that are offset from each other with either a constant or variable voltage difference in response to the pedal travel. By design, diagnostic trouble codes (DTCs) are set if one of the sensor voltages goes out of its allowable range, or if the two sensors fail to track each other as designed. When a DTC related to the accelerator pedal is set, the vehicle is put in a “limp mode” [9], “reduce engine power mode” [10], or “limited capacity” mode [11] designed to prevent the vehicle from accelerating to highway speeds.

For the 2005 Mustang and the 2006 Explorer, the accelerator employs three independent potentiometers that provide a variable resistance to three separate inputs of the ECM. One of them produces a voltage that decreases as the accelerator pedal is depressed. The other two signal voltages increase with parallel slopes as the accelerator pedal is depressed. The “failsafe mode” [12, 13], designed to prevent the vehicle from accelerating to highway speeds, is triggered by invalid inputs from two or three pedal
position sensor inputs. If only one input is invalid, the ETC system will continue to work with the inputs from the other two sensors.

The relationships between APP signals at all pedal positions were measured on accelerator pedals from each of the investigated vehicles and are plotted in Fig. 1.1. For the Mustang and Explorer, the points plotted are for the two sensors with a positive slope. In this plot, the APP signal that is always larger than the other one is designated APP signal 1 and the other one is designated APP signal 2.

![Diagram](image_url)

Fig. 1.1. Nominal operational lines with APP signal 1 and APP signal 2.

The slope of the lines in Fig. 1.1 is 1:2 for the 2008 Sierra and the 2001 Jetta. For the other investigated vehicles, the slope is 1:1 and there is a set offset between APP signal 1 and APP signal 2. The offset is about 0.4 V for the 2005 Mustang and the 2006 Explorer,
and about 0.8 V for the 2005 Camry. If the two APP sensor signals were to lose their independence (e.g. become connected to each other through a fault resistance), they would take on values closer to the dashed line in Fig. 1.1. The area of the plot in the upper right corner represents APP signal values capable of opening the throttle widely. A major advantage of the 1:2 slope interface is that faults that tend to tie the two APP inputs together create APP signals that are very different from valid APP inputs capable of opening the throttle widely. AP-to-ECM interfaces that employ a constant offset (i.e. a 1:1 slope in Fig. 1.1), might be vulnerable to faults that form a connection between APP1, APP2 and a positive power supply voltage. This type of fault could potentially signal the ECM to open the throttle.

The ECM and its sensors are powered by voltages derived from the +12-volt supply using various DC-to-DC converters and linear voltage regulators. One or more of these supply voltages are employed by the AP-to-ECM diagnostic interface. A representative AP-to-ECM architecture with two supply voltages is shown in Fig. 1.2. In this figure, VC supplies power to the CPU that digitizes the APP signals and interprets the information to control the throttle position accordingly. VS1 and VS2 are power supplies for the APP sensors. VM supplies power to an always-on memory that stores the DTCs when the ignition switch is turned off. With the exception of the Jetta, the vehicles in this study lost all DTCs stored in this memory when there was a momentary dip in the voltage, VM. In the Jetta, the DTCs are stored in a non-volatile memory. The battery voltage, VB, is the ultimate power source for all of the other power supplies. On the 2005 Camry ECM; VS1, VS2 and VC are electrically the same supply voltage. On the 2005 Mustang and the 2006
Explorer, VS2 is shorted to VS1 but independent from VC. On the ECMs of the 2008 Sierra and the 2001 Jetta, all three of these 5-V power supplies are independently derived (i.e. shorting one of them does not affect the voltage on the others).

Fig. 1.2. Power supplies of the AP-to-ECM diagnostic interface.

III. MEASUREMENTS

A. Test Setup

Evaluations of the AP-to-ECM interface diagnostics for each vehicle model were conducted using an ETC system simulator (Fig. 1.3). The setup consists of an ECM, a throttle body, a 12-V power supply, a test circuit including two relays and a MOSFET, a USB-based OBD tester, a signal generator, a data acquisition device (DAQ) and an external (upper) computer that controls the OBD tester and the DAQ. The ECM and the throttle body on the test bench are identical to those parts for the investigated vehicle. The power supply functions as the vehicle battery. The input signals from the APP sensor to the ECM are simulated using two or three analog output ports of the DAQ and are controlled using
LabVIEW software. The simulator recognizes and records accelerator pedal related DTCs with the OBD tester. The throttle position is determined by analyzing the recorded throttle position sensor signals (TP1 and TP2). The power relay 1 is used to simulate the ignition switch. The power relay 2 is used to momentarily short VM to the ground of the power supply when the power relay 1 is switched off.

Fig. 1.3. ETC system simulator.
Test circuits used to momentarily short the power supplies are shown in Fig. 1.4. A pulse controlled by the signal generator drives the gate of a MOSFET. A 1-Ω resistor is used to limit the current drawn from the 12-V power supply during a power dip. The control pulse is triggered by a signal from the DAQ, which coordinates the test procedure and produces one dip per test cycle. Table 1.2 lists the dip durations for different power supplies on the ECMs. The power dip durations for VC and VB are set to be long enough to reset the CPU. The power dip durations for VS1, VS2 and VM are the same as the duration for VC on a given vehicle.

![Power dip test circuit for VC, VS1, VS2 and VM.](image)

![Power dip test circuit for VB.](image)

Fig. 1.4. Power dip test circuits.
Table 1.2. Power dip durations

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<th>2008 Sierra</th>
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<td>20 μsec and 120 μsec</td>
<td>50 μsec</td>
<td>50 μsec</td>
<td>50 μsec</td>
</tr>
<tr>
<td>VS1</td>
<td>not applicable</td>
<td>50 μsec</td>
<td>50 μsec</td>
<td>50 μsec</td>
</tr>
<tr>
<td>VS2</td>
<td>not applicable</td>
<td>not applicable</td>
<td>50 μsec</td>
<td>50 μsec</td>
</tr>
<tr>
<td>VM</td>
<td>20 μsec and 120 μsec</td>
<td>50 μsec</td>
<td>50 μsec</td>
<td>50 μsec</td>
</tr>
<tr>
<td>VB</td>
<td>13.2 msec</td>
<td>15 msec</td>
<td>15 msec</td>
<td>15 msec</td>
</tr>
</tbody>
</table>

B. **Test procedures**

All possible voltages between 0 V and 5 V (in increments of 0.1 V) that the APP signals might exhibit were simulated using the ETC simulator. This data was used to generate a diagnostic map illustrating the response of the ETC system to these valid or invalid APP signals. The invalid APP signal combinations represent the effect of some type of electrical fault in the interface. The timing of these faults can affect the system response. Three types of fault injection tests were conducted that introduced the fault at different times. The flow charts in Fig. 1.5 and Fig. 1.6 provide block diagrams of the LabVIEW algorithms for one cycle of testing. Each cycle generates one data point on the diagnostic maps. At the completion of each cycle, new values for the APP1 and APP2 voltages are set and a new cycle is started. This is repeated until all combinations of APP1 and APP2 voltages have been evaluated. As indicated in Fig. 1.5 and Fig. 1.6, a cycle starts by momentarily disconnecting the power supply to erase the DTCs and any diagnostic information caused by previous test cycles. For the 2001 Jetta, where the DTCs are stored in non-volatile memory, the OBD tester was used to clear the DTCs.

As indicated in Fig. 1.5, simulations of two engine on/off cycles are incorporated in each test cycle. The first engine on/off cycle simulates starting the engine with no pedal
application, then depressing and releasing the pedal before turning the engine off. The purpose of the first engine cycle simulation is to allow the ETC system to “learn” the pedal voltages and make any adjustments that it would normally make. The APP voltage combinations being evaluated are introduced during the second engine on/off cycle (Type I test) or immediately before the second engine on/off cycle (Type II test). Except when demonstrating an adaptation of the diagnostic map to different foot-off positions, all Type I and Type II diagnostic map tests in this paper use the nominal foot-off position voltages and the nominal operational lines shown in Fig. 1.1.

The Type III diagnostic map tests are described by the flow chart in Fig. 1.6. This simulates a condition where the APP signal fault is introduced after a reconnection of the battery and before the first engine cycle. This models the behavior of the diagnostic interface in response to faults that occur after the information in the memory is lost. A power dip was applied after the introduction of APP signal inputs consistent with a fault. Each dip effectively shorts the power supply being tested, causing the voltage to drop from its nominal value to a very small value during the presence of the dip. A time delay of up to 10 seconds was provided after each block in Fig. 1.5 and Fig. 1.6 to allow the ECM to respond to the inputs from the simulator.
Set APP signals to foot-off values

Turn on then turn off the power relay 2

Turn on the power relay 1

Simulation of pedal application

Turn off the power relay 1

Set APP signals to the test point

Record TP signals and APP related DTCs

Turn off the power relay 1

Log data

Test cycle end

For type II diagnostic map only.

For type I diagnostic map with the power dip test only.

For type I diagnostic map.

Fig. 1.5. Flow chart for Type I and Type II diagnostic map tests (including the power dip tests).

Test cycle start

Set APP signals to the test point

Record TP signals and APP related DTCs

Turn on then turn off the power relay 2

Turn on the power relay 1

Log data

Test cycle end

Fig. 1.6. Flow chart for the Type III diagnostic map test.
IV. RESULTS AND DISCUSSION

A. Diagnostic maps

A Type I diagnostic map for the 2005 Camry is shown in Fig. 1.7. A green box indicates that no DTCs were generated in response to the deviation in accelerator pedal signal voltages. A yellow box indicates that a DTC was set indicating a conflict between the APP1 and APP2 sensor voltages. Generally, this DTC will put the vehicle into a limp mode. An orange box denotes a test point with other AP-related DTCs. A box with a cross indicates a wide open throttle (WOT) for this point. A wide open throttle is defined in this study as more than 50% of the maximum throttle opening. A round black mark and a black line indicate the foot-off pedal voltages and operational voltages used to simulate pedal applications before the fault was injected. All of the diagnostic maps in this paper use similar symbols and conventions.

As seen in Fig. 1.7, there is some flexibility in the allowable APP signal voltages. The green data points form an operational lane with a width of about 0.4 V. A Type II diagnostic map for the 2005 Camry is shown in Fig. 1.8. Comparing this map with the Type I diagnostic map in Fig. 1.7, the operational lane is much wider and extends to the area where the two signals are nearly equal. As seen in Fig. 1.9, a Type III diagnostic map for the 2005 Camry also has a wide operational lane. The WOT area of the Type III diagnostic map is much larger than those of the Type I diagnostic map and the Type II diagnostic map. The wide operational lane in the Type III diagnostic map implies that, when the information in the volatile memory is lost, the ETC system is much more tolerant of deviations from the nominal operational line.
Fig. 1.7. Type I diagnostic map for the 2005 Camry.

Fig. 1.8. Type II diagnostic map for the 2005 Camry.
Fig. 1.9. Type III diagnostic map for the 2005 Camry.

The diagnostic maps in Fig. 1.7 to Fig. 1.9 were tested with foot-off APP signal voltages of 1.6 V and 0.8 V. In the 2005 Camry, the diagnostic map changed depending on the foot-off voltages detected at start-up. The diagnostic map in Fig. 1.10 shows an example of the map adaptation to a foot-off position in an extreme situation. As a result of the adaptation, the operational lane shifted to include the region where the APP signal 1 voltage was nearly equal to the APP signal 2 voltage. In this circumstance, a resistive fault between APP1 and APP2 could be difficult to detect.

For the 2005 Camry, as seen on the maps from Fig. 1.7 to Fig. 1.10, the APP signal 1 voltage can be as high as the 5-V reference voltage. Thus, a resistive fault between APP signal 1, APP signal 2 and the reference voltage can potentially result in a wide open throttle.
Fig. 1.10. Adaptation of the Type I diagnostic map for the 2005 Camry (foot-off position: APP1 = 1.15 V and APP2 = 0.7 V).

For the 2005 Mustang and the 2006 Explorer with three APP signals, diagnostic maps were generated with APP signal 3 held to constant voltages of 0, 1, 4 and 5 volts. The maps obtained with APP signal 3 at 1 volt are shown in Fig. 1.11 and Fig. 1.12. The P2104 DTC indicated in the maps triggers a failsafe mode. This mode is intended to put the engine in a high forced idle when two or three APP signals are invalid. In Fig. 1.11, other than the operational lane along the nominal operational line, there are two additional lanes without DTCs. In these areas, either APP signal 1 or APP signal 2 associated with APP signal 3 represent two valid inputs to the ECM. In Fig. 1.12, the Type I diagnostic map of the 2006 Explorer has a slightly narrower WOT lane with a 0.1-V difference along the operational line compared to the 2005 Mustang. Only a very limited area on the diagnostic map of the 2006 Explorer does not lead to a DTC. This indicates that most
resistive faults will be detected and generate a DTC even if they do not put the ETC system in a failsafe mode. A Type II diagnostic map and a Type III diagnostic map do not show any significant differences relative to the Type I diagnostic map for either the 2005 Mustang or the 2006 Explorer.

Fig. 1.11. Type I diagnostic map for the 2005 Mustang (APP signal 3 = 1 V).
Fig. 1.12. Type I diagnostic map for the 2006 Explorer (APP signal 3 = 1 V).

An adaptation of the diagnostic map to a deviated foot-off pedal position was also found for the 2005 Mustang. As seen in Fig. 1.13, a wide open throttle is observed in response to voltages in a wider operational lane with the presence of a P2104 DTC. The P2104 DTC is supposed to trigger a failsafe mode, which prevents the throttle from opening widely. This result shows that an indication of a failsafe mode as represented by the P2104 DTC is not consistent with the behavior of the ETC system in this mode, where the throttle should be prevented from a WOT. The diagnostic map of the 2006 Explorer also adapts to a deviation in the foot-off position, as shown in Fig. 1.14. The Explorer map has a narrower operational lane and no test points can open the throttle widely in the presence of a P2104 DTC. However, a similar diagnostic map generated with the APP3 fault voltage set to 1 V,
as seen in Fig. 1.15, shows that there are still some test points (when the APP1 voltage is 3.8 volts) that can open the throttle widely with the presence of a P2014 DTC.

Fig. 1.13. Adaptation of the Type I diagnostic map for the 2005 Mustang with APP3 = 0 V during fault injection (foot-off position: APP1 = 1.3 V, APP2 = 1.1 V, APP3 = 4.0 V).
Fig. 1.4. Adaptation of the Type I diagnostic map for the 2006 Explorer with APP3 = 0 V during fault injection (foot-off position: APP1 = 1.3 V, APP2 = 1.1 V, APP3 = 4.0 V).

Fig. 1.5. Adaptation of the Type I diagnostic map for the 2006 Explorer with APP3 = 1 V during fault injection (foot-off position: APP1 = 1.3 V, APP2 = 1.1 V, APP3 = 4.0 V).
The 2008 Sierra Type I diagnostic map is shown in Fig. 1.16. A P2138 DTC as shown with a yellow box denotes a correlation check failure between the two APP sensor signals. As seen in the figure, the operational lane without DTCs is much narrower than the lanes on the Type I diagnostic maps for the 2005 Camry and the 2005 Mustang. There is a big rectangular area in the upper right representing pairs of signal voltages that can open the throttle widely. This appears to be a significant weakness in the interface. However, it is worth noting that the 1:2 slope and the narrow operational lane makes it difficult for a resistive fault to form without generating a DTC and putting the vehicle in limp mode. As described at the end of this section, the Sierra was the only vehicle in this study that would not come out of a limp mode without returning the pedal sensors voltages to their foot-off position values.

The Type II diagnostic map for the 2008 Sierra is the same as its Type I diagnostic map. The Type III diagnostic map, as seen in Fig. 1.17, has a parallel operational lane along the nominal operational line and is slightly wider in the lower part. In the Type II and Type III diagnostic map tests, the throttle did not respond to any APP signal inputs. This was also confirmed by vehicle-level testing of a 2008 Sierra (parked). Starting the engine, when the accelerator pedal was depressed and held in position, did not result in an increase in the engine speed above idling. A slight adaptation of the Type I diagnostic map to a deviated foot-off position was also observed for the 2008 Sierra. However, it had little effect on the operational lane or the throttle response and no wide open throttle was observed if there was a related DTC.
Fig. 1.16. Type I diagnostic map for the 2008 Sierra.

Fig. 1.17. Type III diagnostic map for the 2008 Sierra.
The Type I diagnostic map for the 2001 Jetta is shown in Fig. 1.18. A P0226 DTC with a yellow box shown in the map denotes a correlation check failure between two APP sensor signals. The map is similar to the Type I diagnostic map for the 2008 Sierra but slightly wider in the operational lane. In the Jetta, APP signal 2 is not allowed to take on values close to the reference voltage.

No significant differences from the Type I diagnostic map in Fig. 1.18 were found in the Type II and Type III diagnostic maps. A slight adaptation of the Type I diagnostic map to a deviated foot-off position was observed for the 2001 Jetta; however it had little effect on the operational lane or the throttle opening.

![Type I diagnostic map for the 2001 Jetta.](image)

Fig. 1.18. Type I diagnostic map for the 2001 Jetta.
In addition to the diagnostic map tests above, a test related to the recovery from a limp mode was performed on the investigated vehicles. With the engine running, an APP signal fault was introduced triggering each vehicle into a limp mode. The fault was then removed while the engine was still running. For all of the vehicles investigated in this study, the throttle responded normally to the accelerator pedal input with DTCs still in the memory after the engine was shut down and restarted. In other words, even though DTCs related to the AP-to-ECM interface were still present, none of the vehicles evaluated would stay in limp mode if the ECM perceived a valid pedal input and the engine was restarted. This finding was significant, since power dips that normally occur while driving can reset the ECM without actually stopping the vehicle. In four of the vehicles in this study, a vehicle in limp mode could have its throttle open if, at any point while driving, the APP voltages took on values consistent with a depressed accelerator pedal and the ECM was reset. This was not a concern with the 2008 GMC Sierra. In the Sierra, the throttle could only be opened when the APP voltages at start-up were consistent with a foot-off pedal position.

B. Effect of power dips on the diagnostic maps

A momentary power dip can be caused by a variety of naturally occurring events such as short-circuit failures of electrical components, momentary increases in the current drawn by electric loads, or noise coupled from other systems or the environment. A power dip is more likely to occur on a supply voltage powering components off the board through a wire-harness. In this section, the effects of power dips on the AP-to-ECM diagnostic
interface are described. To produce these dips, a momentary short is applied between the tested power supply and the battery ground of the ECM.

On a 2005 Camry ECM, two dip durations of 20 \( \mu \)sec and 120 \( \mu \)sec on the CPU’s power supply (VC) were evaluated. The result of applying 20-\( \mu \)sec dips on the CPU’s power supply is shown in Fig. 1.19. The diagnostic map is the same as the Type I diagnostic map in terms of the DTC status. However, the throttle continues to respond to voltages in a wider operational lane allowing for the possibility at a wide open throttle could occur even in the presence of a P2121 DTC. Applying 120-\( \mu \)sec dips on the CPU’s power supply produced the same results as the 20-\( \mu \)sec dips.

Power dip durations of 20 \( \mu \)sec and 120 \( \mu \)sec on the memory’s power supply (VM) on the 2005 Camry ECM were also evaluated. Applying 20-\( \mu \)sec dips on the memory’s power supply produced the same result as applying 20-\( \mu \)sec dips on the CPU’s power supply as seen in Fig. 1.19. The result of applying 120-\( \mu \)sec dips on the memory’s power supply is shown in Fig. 1.20. The operational lane with no APP related DTCs is significantly widened and almost extends to where the APP signal 1 voltage equals the APP signal 2 voltage.

A 13.2-msec dip test on the 12-V power supply (VB) on the 2005 Camry ECM was evaluated. The result of applying 13.2-msec dips to the 12-V supply was similar to the results in Fig. 1.19. It is important to note that the power dips that resulted in the diagnostic map in Fig. 1.19 were also capable of bringing the vehicle out of a limp mode.
Fig. 1.19. Type I diagnostic map following 20-μsec power dips on the CPU’s power supply (VC) on the 2005 Camry ECM.

Fig. 1.20. Type I diagnostic map following 120-μsec power dips on the always-on memory’s power supply (VM) on the 2005 Camry ECM.
Testing of power dips with the durations listed in Table 1.2 was also performed on other ECMs. Other than the 50-μsec power dip test on the always-on memory’s power supply (VM) on the 2005 Mustang ECM, no significant differences were found between diagnostic maps with and without a power dip. For the 2005 Mustang, a 50-μsec power dip on the always-on memory’s power supply sometimes generated more DTCs and disabled the throttle response.

C. Operational lanes

Table 1.3 lists the widths of the operational lanes in the diagnostic maps of four of the vehicles evaluated. The 2006 Explorer had operational lanes similar to the 2005 Mustang and is not listed separately. The lane width is defined as the voltage range for an APP signal without any DTCs or with a WOT along the nominal operational line when the other APP signal is set to a fixed value. It rules out low and high voltages on the boundaries of a diagnostic map. The width of the lane may vary along the operational line. Thus, it refers in particular to the width in the main part of the lane and close to the WOT area. As seen in Table 1.3, the lane width is very consistent for low UA rate vehicles. For the 2005 Mustang, the lane width is consistent except for the adaptation of the diagnostic map to a deviated foot-off position. The diagnostic maps for the 2005 Camry are much more inconsistent in terms of the width of the operational lane, and the wider operational lane is as more than twice as wide as the lanes of the other vehicles.

The number of test points without DTCs and with a WOT on the diagnostic maps are plotted in Fig. 1.21. As seen in the figure, the throttle is capable of being opened widely with DTCs after a certain power dip for the 2005 Camry. Significant variations of the
operational areas can be observed for the 2005 Camry. The non-DTC and WOT areas for
the other vehicles in different test situations are much more consistent.

<table>
<thead>
<tr>
<th>Diagnostic map</th>
<th>APP Signal</th>
<th>2005 Camry</th>
<th>2005 Mustang</th>
<th>2008 Sierra</th>
<th>2001 Jetta</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type I</td>
<td>1</td>
<td>0.7 V</td>
<td>0.4 V</td>
<td>0.5 V Max.</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Type II</td>
<td>1</td>
<td>1.6 V</td>
<td>0.4 V</td>
<td>0.5 V max.</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Type III</td>
<td>1</td>
<td>1.6 V</td>
<td>0.4 V</td>
<td>0.5 V</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Power Dip on VC</td>
<td>1</td>
<td>0.7 V w/o DTC and 1.6 V w. WOT</td>
<td>0.4 V</td>
<td>0.5 V max.</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Power Dip on VS1</td>
<td>1</td>
<td>-</td>
<td>0.4 V</td>
<td>0.5 V max.</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Power Dip on VS2</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>0.5 V max.</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Power Dip on VM</td>
<td>1</td>
<td>0.7 V w/o DTC and 1.6 V w. WOT (20-μsec); 1.6 V (120-μsec)</td>
<td>0.4 V</td>
<td>0.5 V max.</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Power Dip on VB</td>
<td>1</td>
<td>0.7 V w/o DTC and 1.6 V w. WOT</td>
<td>0.4 V</td>
<td>0.5 V max.</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V Max.</td>
<td>0.3 V to 0.4 V</td>
</tr>
<tr>
<td>Adaptation to the foot-off position</td>
<td>1</td>
<td>0.7 V</td>
<td>0.3 V w/o DTC and 0.6 V w. WOT</td>
<td>0.5 V</td>
<td>0.7 V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>0.2 V to 0.3 V</td>
<td>0.3 V to 0.4 V</td>
</tr>
</tbody>
</table>
V. CONCLUSIONS

In this study, characteristics of the AP-to-ECM interfaces of five vehicles were evaluated. Three of these vehicle models had a relatively high number of consumer complaints related to unintended acceleration, while the other two had a relatively low
number of consumer complaints related to unintended acceleration. All five vehicles relied on an analog interface employing two or three redundant sensors. Key differences between the models evaluated included:

- Both models with low reported rates of UA employed a 1:2 ratio between the APP1 and APP2 sensor voltages. This makes it difficult for a single shorting fault to emulate a fully depressed accelerator pedal. In vehicles with high reported rates of UA, it was possible to open the throttle with a resistive fault that connected APP1, APP2 and the +5-volt reference in the accelerator pedal interface.

- The models with low reported rates of UA had relatively narrow and rigidly defined operational lanes. The models with high rates of UA had operational lanes that were relatively wide and varied depending on the operational state of the interface.

- In the models with low reported rates of UA, no conditions were observed where a vehicle in limp mode had a wide open throttle. In the vehicles with high reported rates of UA, it was possible to open the throttle even when DTCs that normally trigger a limp mode were set. (It should be noted here that all of the vehicles evaluated could be brought out of limp mode by removing all faults, then turning off and restarting the engine.)

It is impossible to say to what extent, if any, these design differences contributed to the rate of consumer complaints. Nevertheless, some of the design features of the AP-to-ECM interfaces of the vehicles in this study seem to make a great deal of sense. Based
on the results of this study and a review of new technologies and automotive design practices, the authors have the following recommendations related to the design of the AP-to-ECM interface in new vehicles:

- At least one of the sensors in the accelerator pedal should produce a signal that is not a simple DC voltage. Other available technologies include a PWM signal, a signal that periodically takes on a known value, or a digitally encoded signal.
- The two accelerator pedal position sensors should not use the same technology and the same power supply. Identical sensors are vulnerable to the same types of interference and are more likely to fail in the same way at the same time.
- A vehicle that has been put into a limp mode after detecting a problem with the accelerator pedal or throttle position sensors, should not be able to open the throttle under any circumstances. Only a trained mechanic should be able to clear the limp mode after inspecting the affected sensor.
- DTCs related to the AP-to-ECM interface should be stored in non-volatile memory. Power transients or RF interference should never be able to cause the ECM to forget that it was in a fail-safe mode.

REFERENCES


CHAPTER TWO

THE EFFECT OF ELECTRICAL FAST TRANSIENTS ON MULTI-LAYER
CERAMIC CAPACITORS

Dixin Zhang, Todd H. Hubing, Andrew Ritter and Craig Nies

Abstract

This paper investigates the susceptibility of multi-layer ceramic (MLC) capacitors to high-voltage electrical fast transients (EFTs). X7R and NP0 MLC capacitors with a 50-V voltage rating and 0603 package size were tested. X7R capacitors often failed during a spike in the voltage, but exhibited no obvious degradation in the measured insulation resistance at low voltages immediately after the failure. NP0 capacitors usually failed by suddenly shorting and maintaining the short after the failure. With the application of additional voltage spikes, some X7R capacitors exhibited a full recovery in terms of the measured resistance, returning to their initial state. The resistance of an X7R capacitor damaged by an EFT event is a function of the applied voltage. The terminal impedance can be modeled as two diodes in parallel.

I. INTRODUCTION

A. Problem Statement

Multi-layer ceramic (MLC) capacitors are widely used due to their low cost and small size. These capacitors are often used to filter inputs and outputs thus exposing them to electrical overstress. Traditional failure analysis of MLC capacitors focuses on post-system-failure analysis. These studies have helped people to better understand the
characteristics of MLC capacitors and have helped to guide the manufacturing process. However, very few studies have focused on the analysis of capacitor failures that may go unnoticed during the normal operation of a system. Undetected capacitor failures in safety-critical or mission-critical systems can have serious consequences. Therefore, it is important to understand how different types of capacitors are likely to fail, and the electrical behavior that these capacitors are likely to exhibit after a failure.

B. Research Background

Two failure modes of an MLC capacitor are low insulation resistance and degraded capacitance. Low insulation resistance, typically due to shorting between the capacitor plates, is the most common failure mode. When a failed capacitor’s impedance is essentially a short at the system operating voltage, the failure is generally detected by the system. A drop in the insulation resistance from megohms to hundreds of ohms however, might adversely affect the performance of the system without creating a detectable system failure.

Traditionally, the long-term reliability and failure analysis of ceramic capacitors has been based on highly accelerated life testing (HALT). Capacitors are tested in a high-temperature environment with an applied DC voltage. These tests have been used to predict the usable life of capacitors and to establish de-rating rules. In [1], DC voltages as high as 400 V were applied to 50-V capacitors during HALT testing to reduce the qualification time. In these tests, a capacitor was considered to have failed if its leakage current exceeded 100 μA at the rated voltage. Although HALT testing has proven to be an efficient and useful method for evaluating MLC capacitors exposed to high DC voltages and high
temperatures, HALT test results have not been correlated to the reliability of MLC capacitors exposed to electrical fast transients (EFTs).

Studies investigating capacitor failures due to EFTs can be classified into two groups based on the type of circuit used to generate the EFT. In [2], [3] and [4], under-damped series RLC circuits were used to study capacitor failures due to transients caused by voltage steps. In [2], 50-V Z5U barium titanate capacitors were found to fail with step voltages of 250-275 V. The peak failure voltage caused by the ringing of the circuit was 900-950 V. According to the study, these capacitors had a static breakdown voltage between 1030 and 1100 V. The peak current observed during a failure was 26 A. In this study, the failed capacitors behaved like a short circuit, which led to a catastrophic failure in the presence of the DC voltage. In [3], low-voltage pulse steps were applied to NP0, X7R and Z5U capacitors. The step voltage across a 0.1-μF capacitor was 4 V and the current was about 0.75 A. Each capacitor was subjected to approximately 3.6 billion pulses during a 1-hour test and no insulation resistance failure was observed. In [4], a surge step stress test (SSST) was used to investigate failure modes in capacitors of different types including 6.3-V MLC capacitors. The 100-ppm failure step voltages derived from a 2-parameter Weibull fitting method for these capacitors were 10 to 19 times the capacitors’ rated voltage.

Another group of tests employed RC circuits to study the failure of capacitors exposed to voltage surges. In [5], a 100-μsec high-voltage single pulse was applied to capacitors through a resistor that limited the current. The voltage across the capacitor increased linearly until breakdown was achieved. The voltage then dropped to a low
sustained value, which implied that the capacitor had not failed as a short circuit. It was found that there was little correlation between the rated voltage and the breakdown voltage. In [6], a similar RC circuit was used to test the current surge susceptibility of MLC capacitors. Sectioned and polished capacitors with exposed internal structures were tested. The capacitors had a rated voltage of 50 V and capacitances of 0.1 μF or 0.33 μF. A series of 125-V pulses was applied with a maximum peak current of 1 A. A degradation of insulation resistance (by approximately a factor of 10) was observed during the test. This paper described the failure mechanism as the heat-induced local melting of internal electrodes.

C. Broad Impact

A number of test pulses that are presumed to simulate the actual electrical transients in a vehicle are presented in the international standard of ISO 7637-2 and its equivalents. In this widely adopted standard, test pulse 1 with a maximum magnitude of 150 V simulates a situation when an inductive load in parallel with the tested circuit is disconnected. However, the standard has little considerations of the circuit impedance under test, which could result in a great of differences given the same source of interference. It has been demonstrated that in a real world of an automotive application, a complex waveform with voltage magnitudes significantly greater than the ISO standard pulses were measured [8]. Meanwhile, MLC capacitors are widely used in automotive applications as EMI (electromagnetic interference) filters, making these components more vulnerable to the transients. Moreover, the design practices that failed capacitors are considered as either
short or open circuits are too general to represent all failure modes of different types of MLC capacitors.

The study described in this chapter processes focus on characterizing MLC capacitors exposed to electrical overstress (EOS) induced by an LC oscillating circuit. This form of EFT is common in automotive and industrial systems and is typically caused by the interruption of current flowing in an inductance due to the opening of a switch or relay, or a physical break in a current-carrying connection. The findings of this study will help enhance the reliability and safety of automotive electronic systems with proper uses of MLC capacitors in these applications.

II. TEST SETUP AND TEST PROCEDURES

The test setup in Fig. 2.1 was used to apply high-voltage pulses across MLC capacitors while monitoring the applied voltage waveform and then measuring the parameters of the test capacitor. An LCR meter (B&K Precision 879B) was used to measure the capacitance and the equivalent parallel resistance at 1 kHz of the capacitor under test (CUT) between pulses. An oscilloscope and a high-voltage differential probe recorded the voltage across the capacitor during each applied pulse.

During the test, the high-voltage (HV) relay was turned on to establish a steady-state current in the inductor; then the relay was switched off. The collapsing magnetic field in the inductor induced a transient voltage across the capacitor and caused an oscillation in the LC circuit. The amplitude of the transient voltage applied to the capacitor could be controlled by adjusting the initial current through the inductor. During the course of the
testing, the initial current was adjusted to provide just enough energy to cause the capacitor to fail. To determine this initial current value, a trial test was performed for each capacitor of a given type. The frequency of the voltage oscillation was determined by the inductance of the inductor and the value of the capacitor under test.

During the course of a test cycle, Relay 1 and Relay 3 were turned on, and Relay 2 and Relay 4 were turned off. After the voltage across the capacitor died down to an insignificant level, Relay 1 and Relay 3 were turned off, and Relay 2 and Relay 4 were turned on. This allowed the parameters of the capacitor to be measured by the LCR meter.

Fig. 2.1. EFT test configuration for MLC capacitors.
Both X7R and NP0 capacitors with a voltage rating of 50 V and a 0603 package size were evaluated. The test samples included 25 10-nF X7R capacitors, 2 100-nF X7R capacitors, 2 1-nF X7R capacitors, and 25 10-nF NP0 capacitors.

Typical test voltage waveforms for X7R and NP0 capacitors are shown in Fig. 2.2. The X7R waveforms are not perfectly sinusoidal because the capacitance of X7R capacitors changes depending on the applied voltage.

During some of the tests, a spark between the contacts of the HV relay would form as the relay opened. This would diminish the energy stored in the inductor resulting in a lower-amplitude oscillation as indicated by the blue curves in Fig. 2.2.

![Waveform Graphs](image_url)

Fig. 2.2. Typical test voltage waveforms prior to a capacitor failure.
III. THE FAILURE PULSE

A. Signature of a failure pulse

Due to the nature of the test, which repeatedly applied a high AC voltage (10 to 20 times the rated voltage) across the CUT, the exact failure pulse can be difficult to identify. In these tests, capacitor failures were defined in terms of the capacitor’s leakage resistance and the voltage observed across the capacitor during the EFT pulses. If the low-voltage resistance measured after a pulse was less than 1/10 of the initial value, the capacitor was considered to have failed. The average insulation resistances measured at 1 kHz prior to the testing were 15 MΩ for 1-nF X7R capacitors, 1.3 MΩ for 10-nF X7R capacitors, 70 kΩ for 100-nF capacitors, and 70 MΩ for 10-nF NP0 capacitors.

A capacitor was also considered to have failed if the measured peak voltage of an EFT pulse was well below the expected value. For example, in Fig. 2.3, prior to pulse #3736, the resistance measured is not a full order of magnitude lower than its initial value. After pulse #3736, the resistance is 63 kΩ. According to the insulation resistance criteria, the capacitor failed at pulse #3736. However, as indicated in the lower plot in Fig. 2.3, a significant change in the capacitor behavior occurred during pulse #3726. The voltage waveform across the test capacitor is a brief spike and the ringing is over-damped. The capacitor was not able to sustain a high voltage even though its low-voltage insulation resistance was still high.
Fig. 2.3. Voltage waveforms before and after the failure and corresponding capacitance and resistance measurements for a 10-nF X7R capacitor.

B. Failure voltage

The failure voltages for different types of capacitors are described in Fig. 2.4. In this figure, the red line is the median; the upper blue line and the lower blue line are the 75th percentile and the 25th percentile respectively; the upper black line and the lower black line are the extreme values ignoring outliers; and a red cross indicates an outlier. The failure voltage for X7R capacitors decreases with the nominal value of the capacitor, varying from about 0.6 kV for 100-nF capacitors to about 1.3 kV for 1-nF capacitors. 10-nF X7R capacitors have a higher failure voltage than NP0 capacitors with the same nominal
capacitance. It is important to note however, that the capacitance of X7R capacitors decreases with the applied voltage reducing the amount of energy, \( \frac{1}{2}CV^2 \), stored. As a result, more energy is needed to damage NP0 capacitors compared to X7R capacitors with the same nominal capacitance. For example, about 1.8 mJ (stored in the inductor) was required to damage the 10-nF NP0 capacitors compared to just 0.6 mJ for the 10-nF X7R capacitors.

![Failure voltage of capacitors with different nominal values.](image)

Fig. 2.4. Failure voltage of capacitors with different nominal values.

Eight capacitors of each type were evaluated by measuring the dielectric breakdown voltage (DBV) with a slowly ramping voltage. The average DBV for each type of capacitor is plotted in Fig. 2.5. As shown in the figure, higher valued X7R capacitors had a lower
dielectric breakdown voltage. For lower-valued capacitors, the difference between the EFT failure voltage and the DBV is greater than it is for the higher-valued capacitors.

![Graph showing the relationship between average EFT failure voltage and average dielectric breakdown voltage.](image)

**Fig. 2.5.** Relationship of average EFT failure voltage to average dielectric breakdown voltage.

The value of the inductor used in the EFT test affects the resonant frequencies, but does not significantly affect the failure voltage for the various 10-nF capacitors in these tests. **Fig. 2.6** shows the failure voltages for the 10-nF NP0 and X7R capacitors obtained with inductors of different values.
Fig. 2.6. Failure voltage of 10-nF capacitors grouped by value of the test inductor.

The waveform associated with the failure pulse varied depending on the type of capacitor. As shown in Fig. 2.7 (a), the failure of an X7R capacitor appears to occur at or before the first voltage peak. This was typical for X7R capacitors. Of the 22 failure waveforms recorded for NP0 capacitors, only 5 of them failed during the first voltage peak as shown in Fig. 2.7 (b). The other capacitors survived the first voltage peak, which had the highest amplitude, and failed some time later as seen in Fig. 2.7 (c). In one case, the test sample survived the first 4 cycles before shorting at a point where the voltage was at a relatively low level.
IV. FAILURE CHARACTERISTICS

A. Degradation and recovery of post-failure resistance

One of the objectives of this study was to evaluate the degradation of insulation resistance that can occur when capacitors are subjected to high-voltage pulses. Fig. 2.8 shows the range of insulation resistances measured at 1 kHz with the LCR meter after the failure pulse. It indicates that the X7R capacitors generally failed with a resistance higher than 2 kΩ, while the NP0 capacitors failed with a much lower resistance (less than 1 Ω). Only 1 of the 25 NP0 capacitors tested failed with a high resistance (36 MΩ). The measured resistance of most X7R capacitors immediately after a failure was comparable to the measured value before the failure, but degraded quickly with subsequent pulses. X7R
capacitors tended to behave like varistors or diodes after a failure, exhibiting a lower resistance when exposed to high voltages.

Fig. 2.8. Insulation resistance measured after the failure pulse.

The post-failure insulation resistance recovered fully or partially in 5 of the 25 10-nF X7R capacitors during the course of the testing. Fig. 2.9 shows that the insulation resistance of one X7R capacitor fully recovered from pulses #2200 to #2500 and from pulses #3000 to #3800 after the capacitor had failed at pulse #1500. A full recovery means that the measured resistance is at least as high as it was in the measurements before the failure. For NP0 capacitors, a full recovery was never observed. The insulation resistance only recovered partially and briefly as demonstrated in Fig. 2.10.
Fig. 2.9. Recovery of parallel resistance during the pulse testing of a 10-nF X7R capacitor.

Fig. 2.10. Recovery of parallel resistance during the pulse testing of a 10-nF NP0 capacitor.
B. Degradation of capacitance

The capacitance of X7R capacitors was degraded during the course of the testing. Each of the X7R capacitors tested lost more than 10% of its initial capacitance after about 300 pulses. With the continued application of pulses after the failure pulse, four of the 10-nF X7R capacitors lost 90% of their initial capacitance, as seen in Fig. 2.11. For NP0 capacitors, no significant changes in the capacitance were observed during the course of the testing up to the point where a failure was observed. A degradation of capacitance after a failure could not be confirmed for the NP0 capacitors because the NP0 capacitors fail with a very low parallel resistance.

Fig. 2.11. Degradation of capacitance during the pulse testing of a 10-nF X7R capacitor.
C. Destructive physical analysis

Additional samples of 10-nF X7R and NP0 capacitors were tested and sectioned in order to gain insight to the possible causes of the EFT failures. The capacitors tested were soldered to a printed circuit board, subjected to EFT testing, and removed after the test by a hot air tool that increased the temperature gradually to avoid thermal stress. Loose capacitors were then potted in plastic matrix and then slowly ground and polished to expose a cross-section of the internal layers. A control group of capacitors not subjected to EFT testing were mounted and removed from the printed circuit board using the same process. The untested capacitors were also sectioned and did not show any signs of thermal or mechanical stress.

Table 2.1. Results of electrical testing of sectioned capacitors

<table>
<thead>
<tr>
<th>Sample number</th>
<th>Capacitor type</th>
<th>Total pulses</th>
<th>Failure pulse number</th>
<th>Insulation resistance after the failure pulse (DC bias voltage)</th>
<th>Failure voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X7R</td>
<td>3560</td>
<td>70</td>
<td>677 kΩ (8.59 V)</td>
<td>899 V</td>
</tr>
<tr>
<td>2</td>
<td>X7R</td>
<td>56</td>
<td>15</td>
<td>18.4 kΩ (1.55 V)</td>
<td>892 V</td>
</tr>
<tr>
<td>3</td>
<td>X7R</td>
<td>180</td>
<td>172</td>
<td>128 kΩ (5.55 V)</td>
<td>890 V</td>
</tr>
<tr>
<td>4</td>
<td>X7R</td>
<td>5378</td>
<td>174</td>
<td>261 kΩ (7.14 V)</td>
<td>895 V</td>
</tr>
<tr>
<td>5</td>
<td>X7R</td>
<td>483</td>
<td>481</td>
<td>247 kΩ (7.03 V)</td>
<td>863 V</td>
</tr>
<tr>
<td>6</td>
<td>X7R</td>
<td>315</td>
<td>315</td>
<td>374 kΩ (7.79 V)</td>
<td>861 V</td>
</tr>
<tr>
<td>7</td>
<td>X7R</td>
<td>10</td>
<td>10</td>
<td>152 kΩ (5.97 V)</td>
<td>847 V</td>
</tr>
<tr>
<td>8</td>
<td>X7R</td>
<td>9</td>
<td>9</td>
<td>664 kΩ (8.57 V)</td>
<td>867 V</td>
</tr>
<tr>
<td>9</td>
<td>NP0</td>
<td>304</td>
<td>304</td>
<td>&lt;1 Ω</td>
<td>528 V</td>
</tr>
<tr>
<td>10</td>
<td>NP0</td>
<td>99</td>
<td>99</td>
<td>&lt;1 Ω</td>
<td>528 V</td>
</tr>
<tr>
<td>11</td>
<td>NP0</td>
<td>150</td>
<td>150</td>
<td>&lt;1 Ω</td>
<td>551 V</td>
</tr>
<tr>
<td>12</td>
<td>NP0</td>
<td>241</td>
<td>238</td>
<td>&lt;1 Ω</td>
<td>531 V</td>
</tr>
<tr>
<td>13</td>
<td>NP0</td>
<td>172</td>
<td>102</td>
<td>&lt;1 Ω</td>
<td>528 V</td>
</tr>
</tbody>
</table>

The EFT test results are summarized in Table 2.1. The failure resistances of the X7R capacitors were generally more than 100 kΩ with the exception of sample number 2, which exhibited an 18.4-kΩ insulation resistance after failure. Samples #6, #7 and #8 were
removed from the test immediately after the failure pulse. The sections of these capacitors were used to investigate how failures initiate. A section of sample #6 is shown in Fig. 2.12. The red arrows point out tiny cracks that have formed in the dielectric. They may be a) a secondary defect created by a large stress gradient due to the electrostrictive response when the part rapidly deformed during an electrical breakdown and discharge elsewhere within the device, or b) these could be early stages of a primary defect where internal fractures form due to the electrostrictive response and/or adiabatic heating during the fast transient charging. These cracks then provide a breakdown path that effectively reduces the breakdown voltage between the electrodes. The location of the failure site is consistent with the conclusion drawn in [7] that electrical overstress failures are most likely to initiate at the ends of the internal electrodes. These locations have the highest electric field density and experience the greatest mechanical stress under transient voltages. With further pulses applied to a failed X7R capacitor, as seen in Fig. 2.13, severe cracks extended to the surfaces of the failed capacitor and evidence of very high temperatures were found in the interior of the device. High magnification views (esp. 1500x) of the failure region show an annular region around a spherical void formed in the dielectric between metal layers of opposing polarity (light-colored horizontal layers). Inclusions of spherical Ni metal (brighter areas) within the darker gray annulus (barium-rich region based on SEM-EDS analyses) derived from melted barium titanate dielectric provide evidence of extremely high temperatures caused by a spark discharge within the body of the capacitor. It is proposed that the areas of melted dielectric are chemically reduced, and thus contain a high concentration of oxygen-defect charge carriers. The insulation resistance of the failed X7R
capacitor is controlled by the moderate resistance of the severely thermally damaged dielectric between the electrodes. Further, these regions likely are the source of the nonlinear resistance observed in post-EFT IR testing due to the semiconductive behavior of reduced BaTiO3. Continued exposure of the degraded capacitor to EFT pulses causes the damaged areas to be “reworked”, extending the network of thermally induced fractures and melted regions of dielectric/metal. This accounts for the further degradation and the occasional recovery in the insulation resistance during EFT testing.

Fig. 2.14 shows the failure sites of two NP0 capacitors that were sectioned after the initial failure pulse. Both capacitors have a cavity / melted spot at the ends of the internal electrodes, which as noted earlier, is a region of very high electrical stress due to field concentration at the ends of the active electrodes. A parallel crack (as indicated by the red arrows in Fig. 2.14) formed along the internal electrodes associated with the failure spot, showing delamination of the capacitor in response to the point defect created by energy discharged at the end of the associated electrode. This crack is propagated to the exterior of the capacitor as a single planar fracture. In contrast to the X7R capacitors, where annular regions of melted BaTiO3 are observed around the cavity formed during the voltage discharge in the cap, the more refractory zirconate-based dielectric in the NP0 capacitor does not show severe localized melting around the cavity. It is postulated that vaporization and re-deposition of metal on the inner surface of the discharge cavity is the source of the low resistance path between closely spaced layers of alternating polarity in the failed NP0 capacitors.
Fig. 2.12. Cracks at ends of internal electrodes of an X7R capacitor after a failure was observed.
Fig. 2.13. Damage to an X7R capacitor exposed to 5000 pulses after the initial failure.
Fig. 2.14. Failure spots (blue arrows) in NP0 capacitors after EFT pulses. Red arrows indicate a crack along ceramic-electrode interface, originating at the point defect at the high stress margin of termination electrodes.
V. EQUIVALENT CIRCUIT MODEL

A. Circuit model

A plot of the I-V curve of a failed X7R capacitor shows that the insulation resistance is a function of the applied voltage. The resistance decreases with an increase in the bias voltage and is independent of the polarity of the bias voltage. This behavior can be modeled as two identical diodes with opposite polarities in parallel as shown in Fig. 2.15. The relationship between the current and voltage of the circuit can be expressed as,

\[ I = I_S \left( e^{\frac{V}{nV_T}} - e^{-\frac{V}{nV_T}} \right) \]  (1)

where \( I_S \) is the saturation current of one diode, \( V_T \) is the thermal voltage with an approximate value of 26 mV at room temperature, and \( n \) is the emission coefficient. Fig. 2.16 shows how the curve-fit model results compare to the measured I-V curve of a failed X7R capacitor.

![Equivalent circuit of a failed X7R capacitor.](image)
B. Model validation

To evaluate the proposed circuit model of a failed X7R capacitor at frequencies other than DC, the passive low-pass filter circuit illustrated in Fig. 2.17 was measured at room temperature with a failed capacitor and simulated using the two-diode model of Figs. 2.15 and Fig. 2.16. The input voltage was a sinusoidal waveform superimposed on a 4.67-V DC offset.

Fig. 2.18 plots the average voltage across C2 as a function of the peak-to-peak voltage of the applied sinusoidal waveform. At 0 Vp-p, the applied voltage is simply 4.67 VDC. The low insulation resistance of the failed capacitor reduces the output voltage to 3.36 VDC. As the amplitude of the applied sinusoidal waveform is increased, it is partially rectified by the non-linear capacitor impedance. The rectified waveform decreases the average value of the voltage dropped across C2. Higher rectification effects were
observed at lower frequencies. As indicated in Fig. 2.18, the two-diode model simulation results are in close agreement with the measurement results.

Fig. 2.17. Test circuit for validation of the failure model of X7R capacitors.

Fig. 2.18. Comparison between the measurement and the model simulation.
VI. CONCLUSION

The failure voltages and failure modes of X7R and NP0 capacitors exposed to a series of electrical fast transients were analyzed in this paper. Most of the failures for X7R capacitors occurred at the peak of the applied voltage waveform. X7R capacitors with lower capacitances failed at higher voltages. Most of the X7R capacitors tested did not exhibit an obvious decrease in insulation resistance immediately following the failure pulse, though their resistance tended to drop significantly with the repeated application of pulses after the failure. X7R capacitors sometimes recovered their insulation resistance fully or partially during post-failure pulses. More than a 10% degradation in capacitance was commonly observed for X7R capacitors subjected to repeated EFTs. Some X7R capacitors lost about 90% of their initial capacitance during the course of the testing. Cracks were found at the ends of the internal electrodes in a failed 10-nF X7R capacitor when testing was halted after the first indication of a failure. Regions of melted and recrystallized barium titanate are believed to be responsible for the non-linear relationship between the insulation resistance and the applied voltage. Further pulses applied to failed capacitors caused severe cracks and burned the dielectrics.

For a given capacitance (10-nF), NP0 capacitors failed at lower voltages than X7R capacitors. NP0 capacitors often failed as short circuits. NP0 capacitors were less likely to recover with the repeated application of pulses, and recovered only partially and briefly. Capacitance degradation was not observed in NP0 capacitors.

The failure resistance of X7R capacitors showed a nonlinear behavior. Increasing the bias voltage applied on the capacitor decreased the failure resistance. A simple model
of this nonlinear behavior consisting of two identical diodes demonstrated a good fit with measured results.

REFERENCES


CHAPTER THREE

ELECTRICAL BEHAVIOR OF MULTI-LAYER CERAMIC CAPACITORS DAMAGED BY ELECTROSTATIC DISCHARGE

Dexin Zhang, Todd H. Hubing, Andrew Ritter and Kiran Patil

Abstract

The paper investigates the electrical behavior of multi-layer ceramic (MLC) capacitors subjected to electrostatic discharge (ESD). The degradation of MLC capacitors subjected to repeated discharges manifests itself as a non-linear resistance. The leakage current in degraded capacitors increases exponentially with an applied voltage. The I-V characteristics of these capacitors are symmetric with voltage and independent of the polarity of the ESD discharges responsible for the degradation. A model for a degraded capacitor consisting of two parallel diodes with opposite polarities is proposed.

I. INTRODUCTION

A. Problem Statement

Multi-layer ceramic (MLC) capacitors are widely used in electronic devices, especially in automotive electronics due to their high reliability, small size and low cost compared to other types of capacitors. With the increasing demands for a high-level of product integration and component miniaturization, MLC capacitor design is evolving and newer capacitors are made with ceramics that have a higher dielectric constant, higher number of stack layers, increasing overlap area between internal electrodes and thinner dielectric layers [1]. These changes require a renewed focus on the effects of electric
overstress (EOS) such as electrostatic discharge (ESD). Also, the use of these capacitors in safety-critical systems has generated interest in modeling their electrical behavior after a failure has occurred.

B. Research Background

In studies examining the failure of MLC capacitors, efforts have been mainly focused on mechanical overstress (MOS) [2] and highly accelerated life tests (HALT) [3], [4], [5]. During HALT testing, ceramic capacitors experience degradation not only in their capacitance, but also in their insulation resistance due to Schottky barriers formed between the dielectric material and electrodes [6] and oxygen vacancies [7].

ESD is an important consideration when designing any electronic component or device that will perform a safety-critical role. However, the failure mechanisms of MLC capacitors under ESD stress has not been widely documented. There are only a few published studies on this topic. One of these studies, [8], concluded that the rate of failure (defined as not meeting the initial resistance requirements) increases with an increase in the cumulative maximum voltage on the capacitor during tests where charge was not removed from the capacitor between discharges. In this study, 1000 X7R capacitors (0805 1-nF and 1206 10-nF) were exposed to five ESD strikes of each polarity. The authors found no significant difference in failure rates when testing with a human body model (150-pF/1500-ohm) network or a machine model (200-pF/no resistive component). A study described in [9] was a further investigation of [8]. In this paper, continuously increasing voltage pulses were applied to capacitors, until the dielectric broke down and the capacitor became a short circuit. The authors demonstrated factors affecting a capacitor’s
vulnerability to ESD transients by testing capacitors with different voltage ratings, dielectric materials, and package sizes. The authors suggested using NP0 capacitors with high voltage ratings (preferably 200 V) and large package sizes (preferably 1206) for ESD protection.

In [10], an ESD test consisting of 10 discharges followed by another 10 discharges of opposite polarity at a frequency of 10 Hz was used to characterize NP0/X7R MLC capacitors with 50-V or 100-V ratings and packages sizes from 0402 to 0805. Failures were determined by a test sample’s inability to meet capacitance, dissipation factor or insulation resistance requirements. It was found that capacitors with higher voltage ratings outperformed capacitors with lower voltage ratings, and capacitors with larger package sizes outperformed smaller ones. In [11], a degradation in capacitance was observed in tests where the ESD levels were gradually increased from +/- 0.5 kV to +/- 5.0 kV in 0.5-kV increments. In [12], resistive shorts occurred in 0603 MLC capacitors with nominal values of 680 pF and 10 nF subjected to a 15-kV ESD test. That paper proposed a model consisting of a capacitor and a shunt resistor to represent the defective capacitor.

The chapter begins by describing the test and measurement procedures used to evaluate the capacitors in this study; then presents failure levels for MLC capacitors from different manufactures. The I-V characteristics of defective capacitors are presented and an equivalent circuit for modeling degraded capacitors is proposed.

C. Broad Impact

ESD events are common phenomena existing between an automobile and its surrounding environment. As plastics and other nonconductive materials are more widely
implemented in automotive applications, it is increasingly easy to accumulate substantial charge levels. An extreme ESD level of 25 kV can be readily generated in an automotive application [14]. With growing demands for vehicle electronics and increasing complexities of these systems, the sensitivities of vehicle components to ESD damages are also increased. Components connected to an input/output port are of a great concern in terms of ESD susceptibilities since they have electrical wires attached and provide paths closed to sources of accumulated electrostatic charges. Meanwhile, capacitors are adopted [15], [16] in automotive applications for ESD protections due to their low costs and compact packages. Since the capacitors are not specifically designed for the ESD protections, it is necessary to study the behavior of those capacitors damaged by ESD events to provide valuable information on how the failures might affect the vehicle performance.

The research in this chapter processes focus on electrical behavior of multi-layer ceramic capacitors damaged by ESD. It demonstrates that MLC capacitors that have failed due to ESD generally exhibit a highly non-linear behavior. The findings of this study will not only help the system design engineers to promote the immunity to ESD events, but also help capacitor manufacturers in the production of capacitors with high ESD capacities.

II. MEASUREMENTS

A. ESD test setup and samples

A human body model ESD stress was applied to MLC capacitors using a 150 pF/330 Ω ESD simulator configured as shown in Fig. 3.1. A contact discharge was
used to minimize the variation of energy passing through the capacitor from one test to another. The capacitors were covered with silicone gel to avoid an air or surface discharge between the terminals of the capacitor. MLC capacitors with rated values of 1 nF, 10 nF and 100 nF were obtained from three manufacturers. All capacitors in this study were Type II X7R capacitors with 0603 packages and 50-V ratings. Tests were conducted on 8 samples of 1-nF and 10-nF capacitors and 3 samples of 100-nF capacitors.

![ESD test setup with capacitor under test covered with silicone gel](image)

**Fig. 3.1.** ESD test setup with the capacitor under test covered with silicone gel.

**B. Measurement procedure**

A contact discharge was applied to the capacitor under test (CUT) starting at a voltage level that was not likely to destroy the test sample. These starting voltage levels were determined by trial tests in which no samples were damaged by a single strike at a given ESD level, for example, +2 kV for 1-nF capacitors. The voltage level was increased in steps of either +1 kV or +2 kV to determine the failure voltage for each capacitor. Table 3.1 shows the test sequence used for capacitors with different nominal values.
Table 3.1. Test sequence for capacitors with different nominal values

<table>
<thead>
<tr>
<th>Step</th>
<th>1 nF</th>
<th>10 nF</th>
<th>100 nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+2 kV</td>
<td>+8 kV</td>
<td>+18 kV</td>
</tr>
<tr>
<td>2</td>
<td>+3 kV</td>
<td>+9 kV</td>
<td>+20 kV</td>
</tr>
<tr>
<td>3</td>
<td>+4 kV</td>
<td>+10 kV</td>
<td>+22 kV</td>
</tr>
<tr>
<td>4</td>
<td>+5 kV</td>
<td>+11 kV</td>
<td>+24 kV</td>
</tr>
<tr>
<td>5</td>
<td>+6 kV</td>
<td>+12 kV</td>
<td>+26 kV</td>
</tr>
<tr>
<td>6</td>
<td>+7 kV</td>
<td>+13 kV</td>
<td>+28 kV</td>
</tr>
<tr>
<td>7</td>
<td>+8 kV</td>
<td>+14 kV</td>
<td>+30 kV</td>
</tr>
<tr>
<td>8</td>
<td>+9 kV</td>
<td>+15 kV</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>+10 kV</td>
<td>+16 kV</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>+11 kV</td>
<td>+17 kV</td>
<td>-</td>
</tr>
</tbody>
</table>

After each test, the DC resistance of the capacitor was measured using an LCR meter. The capacitor was considered to be damaged if the measured resistance was less than 10 MΩ. If it was not damaged, the test was continued at the next voltage level, and this was repeated until the capacitor was damaged. For example, on a 1-nF capacitor, the test was started at 2 kV and incremented in steps of 1 kV until reaching the observed failure voltage level, which ranged from 4 kV to 7 kV. Defective capacitors were connected to a voltage divider circuit as shown in Fig. 3.2. An applied DC voltage was varied from 0 to +60 V while measuring the voltage across and current through the capacitor to obtain the I-V curve. The capacitor was tested in both polarities, with the applied voltage magnitude represented by the waveform in Fig. 3.3. The current flow through the sample determined from the voltage across R2. The voltage was calculated from V1 and V2.
Fig. 3.2. Test circuit for evaluating degraded capacitors.

Fig. 3.3. Applied test waveform from the DC supply.
III. RESULTS AND DISCUSSION

A. ESD test levels to degrade the capacitors

The failure voltage levels corresponding to ESD tests on capacitors with 1-nF and 10-nF rated values from different manufacturers are shown in Fig. 3.4 and Fig. 3.5, respectively. The results indicate consistent failure levels of 4 kV and 15 kV for 1 nF and 10 nF capacitors, respectively, from manufacturer B. For manufacturers A and C, there was some variation in the failure levels. None of the 100-nF capacitors tested were damaged at any level. All of them withstood the maximum 30-kV discharge.

Eight capacitors of each type from the same lots were tested to determine their dielectric breakdown voltage (DBV) using a slowly ramping applied voltage. The results are summarized in Fig. 3.6. 1-nF capacitors had higher DBVs but failed at lower ESD voltage levels than 10-nF capacitors. This is likely due to the fact that a 10-nF capacitor is able to hold more charge at a given voltage level. Thus with the same level of charge injection, the maximum voltage across a test capacitor during an ESD event is lower for larger-valued capacitors. As indicated in Fig. 3.6, there didn’t appear to be any correlation between the DBV and the ESD failure level for capacitors of the same nominal value.
Fig. 3.4. Histogram of contact ESD failure voltage levels on 1-nF capacitors.

Fig. 3.5. Histogram of contact ESD failure voltage levels on 10-nF capacitors.
Fig. 3.6. Comparison between average ESD failure levels and average DBVs.

**B. Destructive Physical Analysis**

Three 10-nF capacitors from manufacturer A that had failed after being exposed to ESD transients were sent for a destructive physical analysis. The analysis involved grinding and polishing sections of these ceramic capacitors in order to identify possible defects in their structure. As indicated in Fig. 3.7, failed capacitors exhibited cracks in the dielectric at the edges of one or more internal electrodes. The locations of the failure sites indicate weak points in the capacitor in terms of electrical and mechanical stress during an ESD strike. This is in line with a simulation result in [13] that demonstrates that the ends of the internal electrodes exhibit the highest electric field density and mechanical stress under applied transient voltages.
Fig. 3.7. Site of an ESD failure in a 10-nF capacitor.
C. Non-linear resistive characteristics

The I-V characteristics of damaged 1-nF and 10-nF capacitors are shown in Fig. 3.8 and Fig. 3.9, respectively. In these figures, a non-linear resistance between the capacitor terminals is observed. The plots are highly symmetric as demonstrated by Fig. 3.10, which overlays plots of the current due to the forward and reverse voltages for two sample capacitors. Comparing Fig. 3.8 and Fig. 3.9, it is also worth noting that the 10-nF capacitors from different manufacturers exhibited very different behavior, but the behavior was consistent for capacitors from any given manufacturer.

![I-V characteristics of 1-nF defective capacitors](image_url)

Fig. 3.8. I-V characteristics of 1-nF defective capacitors.
Fig. 3.9. I-V characteristics of 10-nF defective capacitors.

Fig. 3.10. Symmetric characteristics of the I-V curves.
D. Equivalent circuit of defective capacitors

Considering the exponential increase in current with the increase in applied DC voltage, the behavior of the degraded capacitors can be modeled with a pair of diodes as shown in Fig. 3.11.

![Equivalent circuit of a degraded capacitor](image)

Fig. 3.11. Equivalent circuit of a degraded capacitor.

At very low frequencies, the connection inductance (L) and equivalent series resistance (ESR) are neglected. A large-valued shunt resistor ($R_{\text{leakage}}$) is used to model the initial leakage current (before the capacitor fails). In the degraded capacitor, this resistance can be neglected because the current flowing through the diodes in the model of the degraded capacitor is much higher than the leakage current represented by $R_{\text{leakage}}$. The I-V characteristics of the failed capacitors can then be modeled with two identical diodes. The relationship between the current and the voltage across these diodes can be written as,

$$I = I_S \left( \frac{V}{e^{nV_T}} - e^{-\frac{V}{nV_T}} \right) \quad (1)$$

where $I_S$ is the saturation current of one diode, $V_T$ represents the thermal voltage (with an approximate value of 26 mV at room temperature), and $n$ is the emission coefficient. These
parameters can be readily specified in SPICE diode models. Using a series expansion, Equation (1) can be approximated by eliminating the higher order components to yield,

\[ I \approx \frac{2I_S}{nV_T} V \]  

(2)

Thus, the DC resistance \( R_{0V} \) with a small DC bias voltage applied is,

\[ R_{0V} = \frac{nV_T}{2I_S} \]  

(3)

Fig. 3.12. Curve fit of I-V characteristics for the 10-nF sample capacitor #4.

The coefficients, \( I_S \) and \( R_{0V} \), in the proposed model were derived for the degraded capacitors in this study. Assuming room temperature, the emission coefficient was obtained using Equation (3). The values obtained for the 1-nF and 10-nF capacitors from each manufacturer are provided in Table 3.2 and Table 3.3, respectively. Fig. 3.12, which shows the I-V characteristics of the 10-nF sample #4 from manufacturer C, shows that the model does a good job of fitting the measured data. The root-mean-square error (RMSE), defined
as the square root of the mean square difference between the modeled and measured values, is also listed in the tables. The low values of RMSE indicate good fits of the model with the measurements. From the data in Table 3.2 and Table 3.3, it can be observed that, 10-nF capacitors are more likely to have low fault resistances at a small bias voltage than 1-nF capacitors.

Table 3.2. Model parameters (I_S and R_{OV}), model effectiveness (RMSE) and emission coefficient (n) for 1-nF capacitors

<table>
<thead>
<tr>
<th>CUT</th>
<th>A #6</th>
<th>A #7</th>
<th>A #8</th>
<th>B #5</th>
<th>B #6</th>
<th>B #7</th>
<th>C #4</th>
<th>C #5</th>
<th>C #6</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_S (mA)</td>
<td>0.0477</td>
<td>0.0705</td>
<td>0.0742</td>
<td>0.0394</td>
<td>0.0177</td>
<td>0.0086</td>
<td>0.0244</td>
<td>0.1144</td>
<td>0.1466</td>
</tr>
<tr>
<td>R_{OV} (kΩ)</td>
<td>280.0</td>
<td>166.0</td>
<td>176.6</td>
<td>187.1</td>
<td>218.4</td>
<td>463.7</td>
<td>572.2</td>
<td>73.98</td>
<td>51.24</td>
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<tr>
<td>RMSE (mA)</td>
<td>0.0197</td>
<td>0.0074</td>
<td>0.0044</td>
<td>0.0212</td>
<td>0.0757</td>
<td>0.0943</td>
<td>0.0062</td>
<td>0.0139</td>
<td>0.0127</td>
</tr>
<tr>
<td>n</td>
<td>1057</td>
<td>927</td>
<td>1038</td>
<td>584</td>
<td>306</td>
<td>316</td>
<td>1105</td>
<td>670</td>
<td>595</td>
</tr>
</tbody>
</table>

Table 3.3. Model parameters (I_S and R_{OV}), model effectiveness (RMSE) and emission coefficient (n) for 10-nF capacitors

<table>
<thead>
<tr>
<th>CUT</th>
<th>A #7</th>
<th>A #8</th>
<th>A #9</th>
<th>B #4</th>
<th>B #5</th>
<th>B #6</th>
<th>C #4</th>
<th>C #5</th>
<th>C #6</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_S (mA)</td>
<td>0.0381</td>
<td>0.0200</td>
<td>0.1574</td>
<td>0.0737</td>
<td>0.1197</td>
<td>0.0230</td>
<td>0.5942</td>
<td>0.3906</td>
<td>0.5354</td>
</tr>
<tr>
<td>R_{OV} (kΩ)</td>
<td>290.6</td>
<td>503.0</td>
<td>32.60</td>
<td>55.45</td>
<td>39.13</td>
<td>392.2</td>
<td>5.043</td>
<td>7.726</td>
<td>5.044</td>
</tr>
<tr>
<td>RMSE (mA)</td>
<td>0.0122</td>
<td>0.0047</td>
<td>0.0639</td>
<td>0.0621</td>
<td>0.0502</td>
<td>0.0061</td>
<td>0.0458</td>
<td>0.0527</td>
<td>0.1424</td>
</tr>
<tr>
<td>n</td>
<td>877</td>
<td>797</td>
<td>406</td>
<td>324</td>
<td>371</td>
<td>714</td>
<td>237</td>
<td>239</td>
<td>214</td>
</tr>
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IV. CONCLUSION

This paper describes and models the electrical behavior of MLC capacitors degraded by electrostatic discharge. Damaged capacitors exhibited a non-linear insulation resistance that could be accurately modeled using identical parallel diodes with opposite polarity. The proposed model for ESD damaged capacitors can be readily implemented in circuit simulation software and employs diodes with only two extracted parameters.
REFERENCES


