Sub-Bandgap Photon-Assisted Electron Trapping and Detrapping in AlGaN/GaN Heterostructure Field-Effect Transistors

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ABSTRACT

We have investigated photon-assisted trapping and detrapping of electrons injected from the gate under negative bias in a heterostructure field-effect transistor (HFET). The electron injection rate from the gate was found to be dramatically affected by sub-bandgap laser illumination. The trapped electrons reduced the two-dimensional electron gas (2DEG) density at the AlGaN/GaN heterointerface but could also be emitted from their trap states by sub-bandgap photons, leading to a recovery of 2DEG density. The trapping and detrapping dynamics were found to be strongly dependent on the wavelength and focal position of the laser, as well as the gate bias stress time prior to illumination of the HFET. Applying this phenomenon of trapping and detrapping assisted by sub-bandgap photons, red, green, and purple lasers were used to demonstrate photo-assisted dynamic switching operations by manipulation of trapped carriers at the surface of an AlGaN/GaN HFET. A physical model based on band diagrams, explaining the trapping and detrapping behavior of electrons, has been presented.
DEDICATION

This work is dedicated to my friends and family.
ACKNOWLEDGMENTS

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Finally, I thank my parents, my Aunt Robin and Uncle Larry, my grandma, my friends Rutledge and Chris, and all other friends and family members for the love and support they have provided over the last seven years of my university studies. I could not have completed this journey without them!
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CHAPTER 1

INTRODUCTION

Semiconductors have been key to dramatically improving our quality of life over the past several decades, impacting virtually every aspect of human life, including computing, healthcare, industrial automation, vehicular transport, and defense. Due to the rapid and continuous improvements in semiconducting devices, complex functionalities such as data handling, storage and processing are now possible over micro and even nanoscale chip areas, leading to unprecedented advancements in a myriad of different systems and applications. Semiconducting devices, representing more than half a trillion-dollar market, are ubiquitous, from portable electronics such as cell phones and computers, to power rectification/regulation circuits powering electric vehicles and the appliances in our homes. III-nitride semiconductors, in particular, have revolutionized the optoelectronics industry. Due to the uniquely broad bandgap engineering capabilities of III-nitride compounds, green, blue, and UV wavelength emission (and detection) was made possible. The realization of the blue LED was even rewarded with the Nobel Prize in 2014. In addition to optoelectronics, nitride based High Electron Mobility Transistors (HEMTs), a subclass of Heterostructure Field-Effect Transistors (HFETs), have successfully shown their potential for high-frequency and high-power electronics, with many such devices seeing commercial and military use in applications requiring high power at microwave frequencies. In this chapter, the material advantages which make III-
nitrile transistors suitable for such applications will be reviewed in detail. Additionally, an overview of the topics covered in this thesis will be given.

1.1 Advantages of WBG Semiconductors

Owing to its high abundance, low cost, and matured, convenient processing methods, silicon has dominated the semiconductor industry for many decades, and has seen at least experimental use in just about every conceivable application. However, silicon is not the ideal semiconductor for fast, high-power, high-temperature operation [1 – 4] due to its inferior material properties compared to wide-bandgap (WBG) semiconductors. With a bandgap of only 1.12 eV, it is relatively easy to thermally generate carriers within the material, making devices susceptible to leakage, and causing reliability issues at junction temperatures ~200 °C [5]. Furthermore, the poor thermal conductivity of silicon (1.5 W/cm-K) makes cooling a challenge, with cumbersome heatsinks required to optimize performance. Thus, for more than a half-century, WBG semiconductors have been a topic of heavy research due to their superior material properties [1 – 4, 6 – 9] such as high breakdown electric field (E_B), high electron saturation velocity (v_sat), low intrinsic carrier concentration (n_i), and high thermal conductivity, which enable the fabrication of smaller devices with operational capability in extreme environments, and at much higher frequencies and power levels compared to silicon-based devices [1 – 4, 7 – 9]. As a result of this research, silicon carbide (SiC) and gallium nitride (GaN) have emerged as the two frontrunners to eventually replace silicon in the power electronics sector. So far, working transistors with low on-state resistances...
and high breakdown voltages by these materials have been demonstrated in highly
efficient power conversion systems. Within the scope of power converter design, higher
switching frequencies are desirable because they enable the miniaturization of passive
elements (inductors, capacitors, transformers), which easily make up a majority of the
converter weight, and a substantial portion of the converter cost. With WBG devices,
conduction and switching losses in converters are reduced, allowing converter design at
higher operating frequencies. So, although the individual WBG switches are several
times the cost of silicon switches of the same rating, a converter with incorporated WBG
switching elements is often cheaper (and lighter) due to the smaller (and thus cheaper)
passive components [10, 11].

From Fig. 1.1 [4] and Table 1.1 [2, 12, 13], we can see how WBG materials such
as SiC and GaN compare to Si. It should be noted that several relevant high
power/frequency parameters scale with the value of bandgap (E_g). For example, E_B
approximately scales with the square of E_g. Consequently, the E_B of GaN (3.3 MV/cm) is
roughly ten times larger than that of Si (0.3 MV/cm). As a result, unipolar GaN devices
will have lower specific on-resistance (R_{on,sp}), and thus can be made smaller than silicon
devices while maintaining the same rated breakdown voltage (V_B). Eq. (1.1) gives the
formula for ideal specific on-resistance.

\[
R_{on,sp} = \frac{4V_B^2}{\varepsilon_r \varepsilon_0 \mu_e E_B} \quad [\Omega \cdot \text{cm}^2]
\]  
(1.1)
where \( \varepsilon_r \) is the dielectric constant, \( \varepsilon_0 \) is vacuum permittivity, and \( \mu_e \) is electron mobility. From the equation it should be clear that higher \( E_B \) gives a lower \( R_{on,sp} \). For a silicon device, having a lower \( E_B \) means that device breakdown voltage will need to be made much lower in order to decrease \( R_{on,sp} \) to the same level as a SiC/GaN device.

Another parameter that scales with \( E_g \) is \( n_i \). One of the many benefits of wide-bandgap semiconductors is low intrinsic carrier concentration, as keeping the thermally generated \( n_i \) far below the engineered extrinsic one is critical for good device control. High-power devices are frequently operated at high temperatures \( T \), and the intrinsic carrier concentration increases exponentially with temperature \( (n_i \propto \exp\left(-\frac{E_g}{2kT}\right)) \). The intrinsic carrier concentrations of silicon \((\sim 10^{10} \text{ cm}^{-3})\) and GaN \((\sim 10^{-10})\) at 300 K differ by 20 orders of magnitude. With a bandgap of 3.42 eV, generation of electron-hole pairs in GaN requires much more thermal energy than in silicon, which is why \( n_i \) for GaN is nearly zero at 300 K. Of course, this enables operation of GaN transistors at much higher temperatures. In fact, GaN reaches the room temperature \( n_i \) of silicon at \( \sim 800 \) °C [14].

![Figure 1.1: Characteristics of Si, SiC, and GaN as they pertain to device applications [4].](image)
Table 1.1: Material properties of Si, SiC and GaN

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<tr>
<th>Properties</th>
<th>Si (----)</th>
<th>4H-SiC (----)</th>
<th>GaN (AlGaN/GaN)</th>
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<tr>
<td>Bandgap (eV)</td>
<td>1.12</td>
<td>3.26</td>
<td>3.42</td>
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<tr>
<td>μ_e (cm²/V·s)</td>
<td>1500</td>
<td>700</td>
<td>900 (2000)</td>
</tr>
<tr>
<td>V_{sat} (×10⁷ cm/s)</td>
<td>1</td>
<td>2</td>
<td>1.5 (2.7)</td>
</tr>
<tr>
<td>2DEG density (cm⁻²)</td>
<td>N/A</td>
<td>N/A</td>
<td>1-2×10¹³</td>
</tr>
<tr>
<td>E_B (×10⁴ V/cm)</td>
<td>0.3</td>
<td>2.2</td>
<td>3.3</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>11.8</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>Thermal Cond. (W/cm-K)</td>
<td>1.5</td>
<td>3.8</td>
<td>1.3</td>
</tr>
<tr>
<td>n_i (cm⁻³)</td>
<td>1×10¹⁰</td>
<td>8×10⁻⁹</td>
<td>2×10⁻¹⁰</td>
</tr>
</tbody>
</table>

Refs: [2, 12, 13]

While the properties of SiC and GaN enable high operating temperatures, it is still crucial to minimize junction temperature to prevent degradation of performance. If junction temperature gets too high, carrier mobility will reduce due to lattice scattering, and if high temperature is sustained for long periods, metallizations such as Schottky and ohmic contacts can be negatively affected. The gate Schottky barrier height, for example, might change, resulting in an undesired change in threshold voltage [8]. This is where silicon carbide outperforms both Si and GaN. With thermal conductivity more than two times higher than both, transfer of heat from the device active regions can be much more
efficient, allowing for maintained peak switching performance at higher temperatures than even GaN devices [9]. On the other hand, GaN, having many of the same WBG advantages as SiC, also has the highest electron mobility and saturation velocity, enabling switching frequencies in the micro-millimeter wave frequency range.

These advantages of WBG materials are measured in two figures of merit for high power devices: the Baliga figure of merit (BFOM) and the Johnson figure of merit (JFOM). Characteristic quantities of power devices are linked to fundamental material properties in both figures of merit, which enables direct material comparisons without the requirement for device fabrication. A power switching device’s BFOM scales with $V_B$ and the inverse of $R_{on,sp}$. BFOM may be expressed in fundamental material properties as a function of the dielectric constant, mobility, and breakdown field.

$$BFOM = \frac{V_B^2}{R_{on,sp}} = \frac{1}{4} \varepsilon_r \varepsilon_0 \mu_e E_B^3$$

(1.2)

The BFOM is an indicator of the impact of semiconductor material properties on drift region resistance [15] and is mainly used to evaluate high-power materials at low frequencies. For high-frequency high-power applications, the JFOM is the more appropriate figure of merit, as it relates the $V_B$ to the cutoff frequency ($V_T$).

$$JFOM = V_B f_T = \frac{E_B \nu_{sat}}{2\pi}$$

(1.3)
Figure 1.2 shows these figures of merit for different materials of interest in the high-frequency and/or high-power regime. Notably, GaN appears as the theoretically superior material over SiC, Si, GaAs, and InP, second only to the ideal semiconductor, diamond.

![Figure 1.2: BFOM (left) and JFOM (right) contours for several semiconductors of interest for high-frequency/high-power switching applications [16].](image)

1.2 Unique Challenges in III-Nitrides and Thesis Overview

Along with the mentioned benefits of III-nitride semiconductors are some unique challenges. In terms of present-day commercial GaN products, device production quality and reliability are greatly limited by the high-cost, and low availability of quality bulk GaN needed for homoepitaxially grown GaN layers [1, 2, 3]. To remain cost-feasible, lateral GaN-based transistors are fabricated via heteroepitaxy (on non-native substrates), most commonly on Si (111), sapphire, or SiC. Due to the thermal and lattice mismatch between GaN and the non-native substrates, strain related defects are present in the epilayers, which can lead to leakage and reliability issues [2]. Another challenge for III-nitrides, which contributes to leakage is the lack of a native oxide that can be
conveniently used as a gate insulator (unlike with silicon). Thus, the only technologically feasible method for FET gate control, is to use a Schottky contact for the gate. Of course, under reverse bias conditions (which are typical for these inherent depletion mode transistors), electrons tunnel through the Schottky barrier and into the connected semiconductor region. This actually posed a significant issue for III-nitride HFETs, especially in the early stages of their development, as electrons would tunnel into surface states near the gate edge, which resulted in the problem of “current slump” or “current collapse” that significantly degraded the performance of these devices at microwave frequencies [17 – 22]. Due to the wide bandgap of GaN, traps can exist at deeper levels (with respect to the conduction band) than in narrower bandgap materials. Meaning that electrons in traps can be relatively difficult to de-trap. The trapped electrons at the surface have a direct impact in reducing the density of carriers in the channel. Obviously, the drain current of the HFET gets strongly impacted by such trapped charges and remains reduced until the trapped charges are neutralized completely.

The objective of this thesis is to report on a performed investigation of these surface/subsurface traps by sub-bandgap ($< E_{\text{g GaN}}$) laser illumination. Reported here is the sub-bandgap photon-assisted emission of electrons from the gate Schottky contact into surface states, as well as the simultaneous emission of electrons from the surface states. Beforehand however, the fundamentals of III-Nitride semiconductors will be reviewed in Chapter 2, which will cover the topics of III-nitride crystal structures, spontaneous and piezoelectric polarization, theory of 2DEG formation, and surface states in AlGaN/GaN HFETs. Chapter 3 will give the preliminary details on the investigation of surface traps
by first showing the layer structure of the AlGaN/GaN HFETs used in the investigation, followed by fabrication steps, the measurement setup, and finally the details of extracted device parameters from I-V characterization. Chapter 4 will give all of the details regarding the nature of the measurements performed and explain all of the depicted transient response data. Chapter 5 will summarize our results, reiterating all key findings, and lastly, will mention our plans for future investigation into this matter.

1.3 Chapter 1 References


CHAPTER 2

III-NITRIDE SEMICONDUCTOR FUNDAMENTALS

This chapter will introduce the fundamental concepts of III-nitride HFETs in order to provide a surface-level understanding of how they function. The coverage includes the crystal structure of III-nitrides, spontaneous and piezoelectric polarization in III-nitride epilayers, 2DEG formation theory, and an introduction to surface states in AlGaN/GaN HFETs.

2.1 Crystal Structure of III-Nitrides

III-nitride compounds (AlN, GaN, InN, and their alloys) can crystallize in three different structures: wurtzite, zinc-blende, and rock-salt. At room temperature and atmospheric pressure, the thermodynamically stable crystal structure for III-nitrides is wurtzite [1]. The zinc-blende structure for III-nitrides can be stabilized by utilizing certain epitaxial growth techniques on cubic substrates [1, 2, 3]. However, due to the natural tendency of III-nitride lattices to form wurtzite, it is quite difficult to grow thick cubic nitride layers with a low fraction of hexagonal inclusions [1, 3]. The rock-salt structure is only stable under high-pressure conditions and cannot be effectively produced under any epitaxial growth method [1]. Thus, the wurtzite form of III-N compounds is used most commonly for practical purposes and will be the structure of focus in this chapter. All three crystal structures are shown below in Fig. 2.1.
Figure 2.1: Three solid polymorphs of III-N compounds: (a) wurtzite, (b) zinc-blende, and (c) rock-salt. The group-III atoms are color coded orange, and the nitrogen atoms are color coded blue. The structural parameters ($a_0$, $c_0$, $u_0$) for the wurtzite unit cell are labeled.

The wurtzite structure of III-nitrides features two interpenetrating hexagonal close-packed (HCP) sublattices, one composed of cations (Al, Ga, In) and the other composed of anions (N). The two sublattices are displaced from each other along the c-axis, by a 3/8 fraction of the HCP unit cell height ($c_0$) [4]. Each group-III atom is bonded to four nitrogen atoms, and vice versa, in a tetrahedral orientation. The primitive cell type is simple hexagonal with a basis of four atoms (2 of each kind). Labeled in Fig 2.1 (a), the wurtzite lattice is characterized by a few structural parameters, which include the length of the hexagonal c-plane edge ($a_0$), the stacking periodicity in the c direction ($c_0$), and the cell internal parameter ($u_0$). The product of $u_0$ and $c_0$ is the cation-anion bond length along the c-axis. The subscript “0” indicates that these values apply under equilibrium conditions. The ideal value of $u_0$ for a wurtzite unit cell is 3/8, and the ideal
The $c_0/a_0$ ratio is $\sqrt{8/3} \approx 1.633$ [4]. These dimensions and ratios for each binary compound are given in Table 2.1. From the table, it can be noted that GaN has the most ideal structure out of the three named compounds.

### Table 2.1: Structural parameters for wurtzite III-nitride binary compounds [5].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ideal</th>
<th>AlN</th>
<th>GaN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_0$ (Å)$^a$</td>
<td>-</td>
<td>3.112</td>
<td>3.189</td>
<td>3.54</td>
</tr>
<tr>
<td>$c_0$ (Å)$^a$</td>
<td>-</td>
<td>4.982</td>
<td>5.185</td>
<td>5.705</td>
</tr>
<tr>
<td>$c_0/a_0$ (exp.)$^a$</td>
<td>-</td>
<td>1.601</td>
<td>1.625</td>
<td>1.6116</td>
</tr>
<tr>
<td>$c_0/a_0$ (cal.)$^b$</td>
<td>1.633</td>
<td>1.619</td>
<td>1.636</td>
<td>1.627</td>
</tr>
<tr>
<td>$u_0$ $^b$</td>
<td>0.375</td>
<td>0.380</td>
<td>0.376</td>
<td>0.377</td>
</tr>
</tbody>
</table>

$^a$Ref. [6], $^b$Ref. [7]

To approximate $a_0$ or for an alloy of these compounds, the Vegard’s Law [8] can be used as in Eq. (2.1), (2.2) and (2.3) for ternary compounds AlGaN and InGaN:

$$a_{0}^{AlGaN} = a_{0}^{AlN} x + a_{0}^{GaN} (1 - x)$$  \hspace{1cm} (2.1)

$$a_{0}^{InGaN} = a_{0}^{InN} y + a_{0}^{GaN} (1 - y)$$  \hspace{1cm} (2.2)

or quaternary compound InAlGaN:

$$a_{0}^{InAlGaN} = a_{0}^{AlN} x + a_{0}^{InN} y + a_{0}^{GaN} (1 - x - y)$$  \hspace{1cm} (2.3)
where $x$ is the mole fraction of aluminum, and $y$ is the mole fraction of indium. The same method can, of course, be applied to approximate $c_0$, and several other crucial parameters to be mentioned in later sections.

Each of these compounds and their alloys are noncentrosymmetric, (meaning they lack inversion symmetry), and are arranged in bilayers, which consist of two closely spaced hexagonal layers, one formed by group-III atoms and the other formed by N atoms. Hence, a wurtzite III-N crystal can be grown in two different polar directions: the [0001] direction having a “group III-face”, or the [000$\bar{1}$] direction having an “N-face”. The “face” refers to the hexagonal atomic layer exposed to the surface. For a GaN crystal, examples of Ga-face and N-face arrangements are shown in Fig. 2.2 [5]. The stacking sequence in the wurtzite structure is AaBbAaBb… along the [0001] direction, or aAbBaAbB… along the [000$\bar{1}$] direction [9] with the most common orientation being the former [5].

Figure 2.2: Crystal structures of Ga-face and N-face wurtzite GaN in their respective [0001] and [000$\bar{1}$] directions [5].
2.2 Spontaneous and Piezoelectric Polarization

Among III-V compounds, III-nitrides have the strongest bond polarity due to the high electronegativity of nitrogen. The bond polarity largely depends on the electronegativity difference (ΔEN) between the two bonded atoms. The bonds for AlN, GaN, and InN are all considered polar covalent (0.3 < ΔEN < 2) [10], meaning that there is a degree of ionicity due to the unequal sharing of electrons between the two bonded atoms. A majority of compounds share this trait to some extent, but compared to other III-V covalent bonds, the metal-nitrogen bond will have the largest ΔEN, and thus the strongest ionicity. Due to the noncentrosymmetric orientation of wurtzite III-nitrides along the c-axis, and the non-ideal \( c_0/a_0 \) ratio of the crystal lattice, the ionicity of these bonds will give rise to macroscopic polarization of the crystal along the [0001] direction. Because this polarization occurs at equilibrium, without any externally applied stress or induced strain, it is called spontaneous polarization \((P_{SP})\) [7, 11].

The ideal \( c_0/a_0 \) ratio of \( \sqrt[3]{8/3} \) is that required for an HCP (and wurtzite) unit cell to be charge neutral. The greater the deviation from this ratio, the greater the strength of polarization, as shown in Table 2.2. To illustrate this, we consider the tetrahedral bond arrangement of III-N compounds. All covalent bonds are equally polar, however, the polarization of the bond parallel to the c-axis opposes the polarization of the other 3 bonds. The total polarization of the tetrahedron is equal to the sum of all polarization vectors. As the \( c_0/a_0 \) ratio decreases, the bottom three covalent bonds move to a wider angle from the c-axis, causing their vertical polarization vectors to decrease. This results in a greater net polarization along the c-axis as shown in Fig. 2.3 (c) and (d). Illustrated in
Fig 2.3 (e) and (f), are the opposite cases where \( c_0/a_0 \) is greater than the ideal value. In this case, we also see a net polarization, but in the direction opposite of the previous case. Having \( c_0/a_0 \) greater than 1.633 is only possible for III-nitrides under non-equilibrium conditions.

Approximation of \( P_{SP} \) for III-N alloys can be accomplished using the same methods from Eq.’s (2.1) - (2.3). Using the \( P_{SP} \) values of AlN, GaN, and InN, linear interpolation can be performed to find \( P_{SP} \) for a III-N alloy if the composition \( (x, y) \) is known [8].

\[
P_{SP}^{AlGaN} = P_{SP}^{AlN} x + P_{SP}^{GaN} (1 - x) \tag{2.4}
\]

\[
P_{SP}^{InGaN} = P_{SP}^{InN} y + P_{SP}^{GaN} (1 - y) \tag{2.5}
\]

\[
P_{SP}^{InAlGaN} = P_{SP}^{AlN} x + P_{SP}^{InN} y + P_{SP}^{GaN} (1 - x - y) \tag{2.6}
\]

**Table 2.2:** Effects of structural non-ideality on \( P_{SP} \) in wurtzite III-nitrides.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ideal</th>
<th>GaN</th>
<th>InN</th>
<th>AlN</th>
</tr>
</thead>
<tbody>
<tr>
<td>( c_0/a_0 )</td>
<td>1.633</td>
<td>1.6259</td>
<td>1.6116</td>
<td>1.6010</td>
</tr>
<tr>
<td>( P_{SP} ) (C/m(^2))</td>
<td>0</td>
<td>-0.029</td>
<td>-0.032</td>
<td>-0.081</td>
</tr>
</tbody>
</table>

Ref: [5]
Figure 2.3: Polarization generated due to non-ideal $c_0/a_0$ ratio shown for tetrahedral bond arrangements with N central atom (a, c, e) and Ga central atom (b, d, f). The vertical components of the bottom three polarization vectors are in opposition with the top polarization vector. When $c_0/a_0$ is ideal, all vectors cancel, and there is no net polarization. When $c_0/a_0$ becomes lower than ideal, the vertical components of the lower three vectors become weaker, which allows polarization from the top covalent bond to dominate. When $c_0/a_0$ is made greater than the ideal value, the opposite effect occurs.

Having a $c_0/a_0$ ratio less than 1.633 ensures that polarization vectors for III-nitride bonds parallel to the c-axis will dominate, giving rise to PSP. However, the direction of PSP has additional dependence on the “face” of the crystal layer. As previously stated, the “face” refers to the hexagonal atomic layer exposed to the surface. III-nitride crystals tend to have polar faces. This means that, for example, if a GaN crystal layer has been grown on a substrate, and gallium atoms are exposed to the surface, then the atomic layer bonded to the substrate will be nitrogen. Under this condition (Ga-face), the direction of
P$_{SP}$ will be towards the substrate [5]. For an N-face layer, the opposite is true, and P$_{SP}$ is directed towards the surface. To understand the direction of P$_{SP}$ for the different layer orientations, we can refer to Fig. 2.4., which features a Ga-face crystal. In this crystal, we single out two interpenetrating tetrahedrons near the surface. These two tetrahedrons are fused such that the central N atom of the first tetrahedron is also the top atom of the second. Because this is a GaN crystal, we can, of course, assume that c$_0$/a$_0$ is less than 1.633, and therefore, polarization vectors for bonds parallel to the c-axis will dominate. Looking at each tetrahedron individually, we see that the top one is an upside-down version of Fig. 2.3 (c), so the direction of P$_{SP}$ is downward. The bottom tetrahedron is the same as Fig. 2.3 (d), so the direction of P$_{SP}$ is also downward. So of course, when the two structures are combined, the polarization vectors will combine in the same direction (down towards the substrate). This combined structure repeats throughout the entire thickness of the crystal layer, so this direction of P$_{SP}$ is maintained. With the example given, it should be easy to visualize how flipping the polar face of the layer to N-face, would flip the direction of P$_{SP}$ towards the surface.

**Figure 2.4:** Direction of P$_{SP}$ in a Ga-face GaN crystal.
Following the previous discussion on lattice non-ideality influencing the strength of $P_{SP}$, one can understand that if the ideality of the III-N lattices were changed externally, dramatic changes in polarization could occur. In practice, this is done intentionally during epitaxial growth processes, where different III-nitride crystals are often layered on top of each other. Up to a certain critical layer thickness, pseudomorphic growth is possible, meaning that the horizontal lattice parameter of the top layer has been forced to match that of the bottom layer. By forcing the layers to match, biaxial strain is developed in the top layer, and both lattice parameters must change in order to accommodate the built-in stress. Applying logic from the previous discussion, this means that polarization will change along the [0001] axis due to the change in $c_0/a_0$. This additional polarization from applied stress/strain is known as piezoelectric polarization ($P_{PE}$) [7, 11], and its direction in a III-N crystal depends on the direction of biaxial stress (tensile or compressive) and the “face” of the grown crystal layer (metal-face or N-face). Below in Fig. 2.5, every such condition is depicted.

From our previous discussion, we understand why $P_{SP}$ points towards the substrate for a Ga-face layer, and towards the surface for an N-face layer. Now we must understand the direction of $P_{PE}$. Let us first examine the Ga-face example in Fig. 2.5 (a), which shows a layer of AlGaN grown pseudomorphic on relaxed GaN. Under relaxed conditions, AlGaN has a shorter horizontal lattice parameter than GaN, so it must be stretched outwards (tensile strain) in order to match the GaN lattice. If stress is applied forcing the lattice to move outward, $c_0/a_0$ is reduced further ($c_0$ decreases, $a_0$ increases) making the polarization vectors for bonds parallel to the c-axis even more dominant.
(working in the same direction as \( P_{SP} \)). Compressive strain does the opposite. Fig. 2.5 (b) gives such an example, where GaN is grown pseudomorphic on AlGaN. In order to match the AlGaN lattice, the GaN crystal must be compressed inward (increasing \( c_0/a_0 \)). This works in favor of the lower 3 bonds in the tetrahedral arrangement [refer to Fig. 2.3 (e) and (f)], increasing the vertical component strength of their polarization vectors. This compressive strain produces polarization which opposes \( P_{SP} \), and if the strain is sufficient, \( P_{PE} \) can cancel-out or surpass \( P_{SP} \). In general, we see from Fig. 2.5 that regardless of the face of the crystal layer, tensile strain helps \( P_{SP} \) and compressive strain works against it.

**Figure 2.5:** Directions of \( P_{SP} \) and \( P_{PE} \) in Ga- and N-face strained and relaxed AlGaN/GaN heterostructures [5].
The strength of PPE along the c-axis in III-nitride wurtzite crystals can be calculated from the following equation [5]:

\[
P_{PE} = 2 \frac{a-a_0}{a_0} \left( e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right)
\]  \hspace{1cm} (2.7)

where \(e_{31}\) and \(e_{33}\) are piezoelectric constants and \(C_{13}\) and \(C_{33}\) are elastic constants in the respective horizontal and vertical directions. Also, \(a_0\) is the relaxed horizontal lattice parameter for the crystal under strain, while \(a\) is the strained horizontal lattice parameter. For a crystal layer grown pseudomorphic on a different crystal layer, the strained lattice parameter of the top layer will be equal to the relaxed lattice parameter of the bottom layer (assuming the bottom layer is relaxed). So, for the example in Fig. 2.5 (a), the value of \(a\) for the top AlGaN layer under strain will equal the value of \(a_0\) for the relaxed bottom GaN layer. All material parameters needed to compute PPE strength are given below in Table 2.3.

**Table 2.3:** List of elastic and piezoelectric constants for wurtzite III-nitrides.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AlN</th>
<th>GaN</th>
<th>InN</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{13}) (GPa)(^a)</td>
<td>108</td>
<td>103</td>
<td>92</td>
</tr>
<tr>
<td>(C_{33}) (GPa)(^a)</td>
<td>373</td>
<td>405</td>
<td>224</td>
</tr>
<tr>
<td>(e_{31}) (C/m(^2))(^a)</td>
<td>-0.60</td>
<td>-0.49</td>
<td>-0.57</td>
</tr>
<tr>
<td>(e_{33}) (C/m(^2))(^b)</td>
<td>1.462</td>
<td>0.727</td>
<td>1.092</td>
</tr>
</tbody>
</table>

\(^a\)Ref. [5], \(^b\)Ref. [12]
For a III-N ternary or quaternary alloy, each of the constants needed in Eq. (2.7) can be approximated using the same methods from Eq.’s (2.1) - (2.6). If the alloy composition \((x, y)\) is known, linear interpolation can be performed to compute the value of the desired material parameter [8].

\[
\begin{align*}
C_{13}^{AlGaN} &= C_{13}^{AlN}x + C_{13}^{GaN}(1-x) \\
C_{13}^{InGaN} &= C_{13}^{InN}y + C_{13}^{GaN}(1-y) \\
C_{13}^{InAlGaN} &= C_{13}^{AlN}x + C_{13}^{InN}y + C_{13}^{GaN}(1-x-y)
\end{align*}
\]

\[
\begin{align*}
C_{33}^{AlGaN} &= C_{33}^{AlN}x + C_{33}^{GaN}(1-x) \\
C_{33}^{InGaN} &= C_{33}^{InN}y + C_{33}^{GaN}(1-y) \\
C_{33}^{InAlGaN} &= C_{33}^{AlN}x + C_{33}^{InN}y + C_{33}^{GaN}(1-x-y)
\end{align*}
\]

\[
\begin{align*}
e_{31}^{AlGaN} &= e_{31}^{AlN}x + e_{31}^{GaN}(1-x) \\
e_{31}^{InGaN} &= e_{31}^{InN}y + e_{31}^{GaN}(1-y) \\
e_{31}^{InAlGaN} &= e_{31}^{AlN}x + e_{31}^{InN}y + e_{31}^{GaN}(1-x-y)
\end{align*}
\]

\[
\begin{align*}
e_{33}^{AlGaN} &= e_{33}^{AlN}x + e_{33}^{GaN}(1-x) \\
e_{33}^{InGaN} &= e_{33}^{InN}y + e_{33}^{GaN}(1-y) \\
e_{33}^{InAlGaN} &= e_{33}^{AlN}x + e_{33}^{InN}y + e_{33}^{GaN}(1-x-y)
\end{align*}
\]
2.3  Theory of 2DEG Formation in AlGaN/GaN HFET Structures

One of the greatest novelties of III-nitride heterostructures is the ability to produce a dense (~$10^{13}$ cm$^{-2}$ [5]), highly mobile (>1000 cm$^2$/V-s [13]) sheet of electrons at the heterointerface, without intentionally doping the layers [5]. This sheet of electrons is called the two-dimensional electron gas (2DEG), and it serves as the channel in AlGaN/GaN HFET structures (see Fig. 2.6). Because this conductive channel exists without an applied bias, inherently, these transistors are depletion mode devices. Electrons in the 2DEG travel in tight confinement along the channel without encountering ionized donor/acceptor atoms. The lack of ion impurity scattering allows for high electron mobility, which can be maintained even at high voltage / temperature, due to the favorable material properties of WBG III-nitrides discussed in the previous chapter.

![Generic AlGaN/GaN HFET layer structure showing the 2DEG at the heterointerface.](image)

**Figure 2.6:** Generic AlGaN/GaN HFET layer structure showing the 2DEG at the heterointerface.
The presence of 2DEG in AlGaN/GaN heterostructures is due to the spontaneous and piezoelectric polarization in the layers. Referring to Fig. 2.7 (a), the impact of \( P_{SP} \) and \( P_{PE} \) can be explained. In this example, we have a conventional Ga-face AlGaN/GaN layer structure with directions of \( P_{SP} \) and \( P_{PE} \) labeled. The bottom GaN layer is relaxed, so there is no \( P_{PE} \) component, only \( P_{SP} \). The top AlGaN layer is pseudomorphic on GaN, so it is under tensile strain (as indicated by the outward arrows) and will consequently have a \( P_{PE} \) component working in the same direction as \( P_{SP} \). Because this is a Ga-face layer structure, all \( P_{SP} \) and \( P_{PE} \) vectors point towards the substrate for reasons previously discussed. Now, we can see there is an obvious difference in polarization between these two layers, and there must be some associated charge density \( \rho \) responsible for the difference (given by \( \rho = -\nabla \cdot \vec{P} \)). In our case, because polarization is always directed along the growth axis (c-direction) for wurtzite III-nitrides, there will be a bound sheet charge \( (\sigma_{\text{int}}) \) formed at the AlGaN/GaN interface as a result of the polarization difference, which can be calculated as follows [5]:

\[
\sigma_{\text{int}} = P_{\text{Total}}(\text{Bottom Layer}) - P_{\text{Total}}(\text{Top Layer})
\]  

\[
\sigma_{\text{int}}^{\text{AlGaN/GaN}} = (P_{SP})_{\text{GaN}} - (P_{SP} + P_{PE})_{\text{AlGaN}}
\]

This bound sheet charge induced by polarization discontinuity will attract compensating mobile charge at the interface. So, if \( \sigma_{\text{int}} \) is positive, compensation charge must be negative, and vice versa. Eq (2.20) gives a general equation for \( \sigma_{\text{int}} \), and Eq.
(2.21) gives our example specific equation. Computation of $P_{SP}$ and $P_{PE}$ has been discussed at length in the previous section. In our case, we can see that $\sigma_{int}$ will be positive, so the mobile compensation charge will be negative electrons [see Fig. 2.7 (b)]. As mentioned, the layers are not intentionally doped, so these electrons originate from “donor-like” traps at the bare surface of the AlGaN barrier [14,15]. Electrons from these traps reach the AlGaN conduction band, and then move to the heterointerface (under influence of electric field), where they cross into the GaN region and accumulate near the interface until thermal equilibrium is achieved (Fermi level constant). This accumulation of electrons causes the GaN conduction band to bend below the Fermi level at the interface, creating a triangular quantum well region, as shown in Fig. 2.7 (c). Electrons within this quantum well are tightly confined, having quantized energy levels in one spatial direction (perpendicular to the interface), but are free to move in the other two. This is the origin of the 2DEG in AlGaN/GaN heterostructures. These “donor-like” traps are neutral when occupied, but positively charged when vacant, thus, said traps are also responsible for compensating the negative polarization charge at the AlGaN surface ($-\sigma_{surf}$) with a positive sheet charge ($\sigma_{com}$) [15], as indicated in Fig. 2.7 (b). If $\sigma_{int}$ were negative (perhaps in a Ga-face InGaN/GaN structure or an N-face AlGaN/GaN structure) then the mobile compensation charge at the interface would be positive, and instead there could be a two-dimensional hole gas (2DHG) at the interface. But this is much less desirable because hole mobility is inherently lower.
Figure 2.7: (a) Directions of $P_{SP}$ and $P_{PE}$ in a conventional Ga-face AlGaN/GaN heterostructure. Bound positive interface charge ($+\sigma_{int}$) is labeled. (b) Sheet charge densities at the surface and interface of an AlGaN/GaN heterostructure. Both fixed and mobile compensation charges are shown. (c) Band diagram of AlGaN/GaN heterostructure showing the 2DEG at the interface. The electric field in the AlGaN region is the consequence of fixed polarization charge. Additionally, due to electron transfer from AlGaN into GaN, at the heterointerface, the GaN conduction band dips below the Fermi level.

Such high 2DEG densities ($n_s \approx 10^{13} \text{ cm}^{-2}$) are achievable in AlGaN/GaN heterostructures, because $\sigma_{int}$ can be made sufficiently dense. From Eq (2.21), we can see this possibility exists mostly due to $P_{PE}$ in the AlGaN layer, which can be made even greater by increasing the Al mole fraction ($x$). Also related to $n_s$ is the conduction band
offset ($\Delta E_C$), shown in Fig. 2.7 (c). By increasing $\Delta E_C$ we increase the “depth” of the quantum well, and of course, a deeper well holds more water (or electrons in our case). Mobility is also consequently improved due to stronger confinement of electrons. $\Delta E_C$ is often approximated as [16, 17]

$$\Delta E_C(x) = 0.7\left[E_g^{AlGaN}(x) - E_g^{GaN}\right]$$  (2.22)

with the AlGaN bandgap ($E_g^{AlGaN}$) measured by Brunner et al. to be [18]

$$E_g^{AlGaN}(x) = E_g^{AlN}x + E_g^{GaN}(1 - x) - bx(1 - x)$$  (2.23)

where the bandgaps of AlN and GaN ($E_g^{AlN}$ and $E_g^{GaN}$) are 6.13 and 3.42 eV, respectively [5]. Additionally, $b$ is the bowing parameter, assumed here to be 1.0 eV [5, 18]. As indicated by Eq.’s (2.22) and (2.23), $\Delta E_C$ increases with $E_g^{AlGaN}$, which increases with $x$. So, by increasing the composition of Al in the AlGaN layer, we increase the fixed positive polarization charge and quantum well depth at the heterointerface, which ultimately increases 2DEG density [5]. The below equation for maximum $n_s$ supports this conclusion, indicating a positive linear relationship with both $\sigma_{int}$ and $\Delta E_C$ [5].

$$n_s(x) = \frac{\sigma_{int}(x)}{q} - \left(\frac{\varepsilon_0 \varepsilon(x)}{d q^2}\right) [q \phi_B(x) + E_F(x) - \Delta E_C(x)]$$  (2.24)
In the above equation, $q$ is elementary electron charge, $\varepsilon_0$ is the permittivity of free space, $d$ is the thickness of the top AlGaN layer, $\phi_B(x)$ is the Schottky-Barrier height at the gate metal / AlGaN interface, $\varepsilon(x)$ is the dielectric constant of the AlGaN layer, and $E_F(x)$ is the Fermi level. Most of these parameters have dependence on $x$. In order to solve Eq.(2.24), we can use a few more approximations for the remaining unknowns. From linear interpolation between AlN and GaN values, $\varepsilon(x)$ [5] and $\phi_B(x)$ [19] can be estimated.

$$\varepsilon(x) = 9.5 - 0.5x \quad (2.25)$$

$$\phi_B(x) = 0.84 + 1.3x \quad (2.26)$$

Fermi energy can be calculated as [20]

$$E_F(x) = E_0(x) + \frac{\hbar^2}{m^*(x)} n_s(x) \quad (2.27)$$

where the ground subband level of the 2DEG is

$$E_0(x) = \left[ \frac{9\pi q^2}{8\varepsilon_0 \sqrt{8m^*(x) \varepsilon(x)}} \right]^{2/3} n_s(x) \quad (2.28)$$
and the electron effective mass is $m^*(x) \approx 0.22m_e$, with $m_e$ being electron rest mass. From Eq. (2.24) we note that $n_s$ can be calculated as a function of Al composition (assuming constant AlGaN barrier thickness), or a function of AlGaN thickness (assuming constant composition). Generally speaking, 2DEG density increases with both barrier layer thickness and Al composition within a certain range as indicated by Fig. 2.8 [5]. There are also lower boundaries for both $d$ and $x$ which must be met in order for the 2DEG to exist at the interface [5, 15]. To an extent, one ($d$ or $x$) can be increased to compensate for deficiency of the other. It should also be noted that Eq. (2.24) is a function of itself, as the embedded Eq.’s (2.27) and (2.28) are both dependent on $n_s(x)$. The solution to such an equation can be found iteratively using a software such as MATLAB.

**Figure 2.8:** 2DEG density at an AlGaN/GaN interface plotted against Al mole fraction [5]. Curves corresponding to different AlGaN barrier thicknesses (10 nm, 20 nm, 30 nm) are plotted on the same graph, showing clear indication of increasing 2DEG density with thickness. Also included for reference, is the curve for fixed polarization interface charge ($+\sigma/q$), obtained by setting the second term in Eq. (2.24) to zero.
2.4 Surface States and Trapping in III-Nitride HFETs

Although surface states are beneficial for III-nitride HFETs in one regard, allowing the 2DEG to be formed without intentional doping, they have also posed a significant problem, especially during the early phases of development for these devices. Under normal operating conditions, electrons from the gate can tunnel into vacant surface states between the gate and drain, causing depletion of the 2DEG [21, 22]. Fig. 2.9 illustrates this phenomenon, showing the gate and drain contacts of an AlGaN/GaN HFET biased under ordinary conditions [negative applied gate-source voltage (V\textsubscript{GS}), positive applied drain-source voltage (V\textsubscript{DS}), which results in a negative voltage from gate to drain by Kirchhoff’s Voltage Law (KVL)]. Under these conditions, a reverse-bias is applied to the Schottky barrier at the gate metal-semiconductor junction, increasing the probability for electrons at the gate edge to tunnel into the conduction band of the exposed top layer. These electrons are then captured by interband surface states near the gate. As electrons accumulate on the surface, electrons in the channel are repelled, causing drain current (I\textsubscript{DS}) to reduce. This accumulation of surface-trapped electrons is often referred to as a “virtual gate”, as it behaves in the same way as a negatively biased metal gate (depleting the channel) [22, 23]. Emission of electrons from these traps is not very fast [21]. So, when the gate bias is removed, many electrons remain in the traps, resulting in significant reduction of maximum drain current until sufficient time is allowed for the surface to neutralize. It has been shown that exposure to super-bandgap light (\textgreater E\textsubscript{G\textsubscript{GaN}}, \textsim 365 nm) will suppress virtual gate formation, as electrons from photo-generated electron hole pairs (EHP) move into the 2DEG, and holes move to the surface,
allowing trapped electrons to recombine [21, 22, 24]. On the other hand, the effects of sub-bandgap illumination on the virtual gate have not been explored to the same extent as super-bandgap and will more or less be the focus of the remaining chapters.

Figure 2.9: (a) Band diagram of reverse-biased Schottky barrier. The dominant conduction mechanisms are labeled ① and ②. Electrons from the gate metal tunnel into the conduction band of the exposed top layer and are captured by interband surface states. (b) A high density of negative charge accumulates at the surface near the gate and repels electrons in the 2DEG.

Due to the long detrapping times, the virtual gate presents an obvious problem, especially for high-frequency (GHz) switching applications, where these HFETs are supposed to excel. With trapped electrons incapable of detrapping from the surface in
between gate pulses, current recovery from the transistor off-on transition is greatly reduced. This phenomenon is known widely as “current slump” or “current collapse” and is easily identifiable from pulsed current-voltage (I-V) measurements, where much lower output power density is observed when compared to static I-V measurements [22, 25] [see Fig. 2.10 (a)]. In the interest of mitigating the current collapse effect, heavy research has gone into methods for passivating the dangling bonds at the exposed surface, which are responsible for interband traps. After surface passivation (with SiNx, AlN or SiO2 [21, 23, 26, 27]), the density of surface states is greatly reduced [23], and electron trapping reduces consequently. This allows for considerable improvement in pulsed output power performance [22, 25], as shown in Fig. 2.10 (a). Fig 2.10 (b) shows an example of an AlGaN/GaN HFET structure with a SiNx surface passivation layer [26].

**Figure 2.10:** (a) Comparison of pulsed and static I-V curves before and after surface passivation [25]. “Knee walk off” and reduction of saturation drain current are shown in the unpassivated curve. (b) AlGaN/GaN HFET layer structure with surface passivation layer [26].
Another method to reduce the effect of current collapse (often used in conjunction with surface passivation) is the addition of a field plate to the gate contact. The field plate reshapes the electric field at the gate edge towards the drain contact, causing a reduction in the peak value [28] [see Fig. 2.11 (a)]. Because the peak electric field at the gate edge has been reduced, fewer electrons are able to tunnel onto the barrier layer surface and become trapped. With this working in tandem with surface passivation, we have fewer field-emitted electrons, and fewer active surface states to receive those electrons, resulting in substantial reduction in current slump behavior [29, 30]. A final benefit worth mentioning is that due to peak electric field reduction, device breakdown voltage is enhanced [28]. Fig 2.11 (b) and (c) show examples of AlGaN/GaN HFET structures with field-plated gates [31].

**Figure 2.11:** (a) Simulated distribution of the electric field along the 2-DEG, directed from drain to source, with and without a field plate [28]. The non-field-plated device is on the verge of breakdown. (b) AlGaN/GaN HFET structure with “integrated” field plate and [31]. (c) AlGaN/GaN HFET structure with “separated” field plate [31].
2.5 Chapter 2 References


CHAPTER 3

DEVICE STRUCTURE AND EXPERIMENTAL SETUP

As previously mentioned, III-Nitride HFETs have been widely researched in the past few decades, in part due to their applications in high power microwave devices [1 – 6]. However, a significant problem faced by these HFETs, was the tunneling of electrons from the gate into surface states, which resulted in the problem of current collapse. As discussed in the previous chapter, the performance of these devices at high frequencies (GHz) is significantly degraded as a result of this phenomenon [7 – 12], with the trapped electrons at the surface having a direct impact in drain current reduction. Although UV illumination nullifies the trapped charges, the influence of sub-bandgap illumination on the dynamics of surface trapping and detrapping can be significant and more interesting. Typically, the effect of sub-bandgap illumination using green and red light has been studied with the intention of mitigating the effect of trapped charges through photo-assisted emission of the electrons from surface traps, without generating holes that can have unintentional side effects on device performance (i.e., enhanced gate leakage current). Although many studies have reported on the emission of trapped electrons using sub-bandgap light, [13 – 15] only a few studies have reported on the impact of sub-bandgap illumination on the gate tunneling current in an HFET [16, 17]. In fact, our group did not find any previous report carefully considering the effect of sub-bandgap illumination on the competing phenomena of electron emission onto the surface (and into
surface states) and electron emission from surface states, both assisted by sub-bandgap photons. The next few chapters will detail our systematic study on the photon-assisted emission of electrons from the gate Schottky contact into surface states, as well as the simultaneous emission of electrons from the surface states. This chapter will show the layer structure of the AlGaN/GaN HFETs used in our experiments, followed by a brief explanation of the fabrication methods. Additionally, a description of our measurement setup, and HFET characterization (I-V) details will be presented.

3.1 AlGaN/GaN HFET Layer Structure and Fabrication

The GaN HFET devices used in our experiments were fabricated as III-nitride epilayers, grown on a Si (111) wafer purchased from DOWA Semiconductor Akita Co., Ltd, Japan. The HFETs were fabricated at the base of microcantilever beams, which had nominal dimensions of 250 × 50 × 1.3 µm [18]. Aside from their placement on microcantilever beams, the HFETs are similar in all aspects to those fabricated conventionally on solid substrates. The layer structure for the HFETs is shown in Fig. 3.1, consisting of a 675 µm Si (111) substrate layer, a 300 nm buffer layer, a 1 µm i-GaN active layer, a 20 nm barrier layer of intrinsic Al$_{0.25}$Ga$_{0.75}$N, and finally a cap layer of 3 nm i-GaN. The AlGaN/GaN mesa has dimensions of 14 × 34 µm. Over many iterations, our group has refined the fabrication process to improve production yield, dependability, and lifespan. All fabrication techniques were carried out at the Georgia Institute of Technology's Microelectronic Research Center (MiRC) in Atlanta, GA.
Figure 3.1: Layer structure for the HFETs used in our investigation on sub-bandgap illumination effects on surface traps. Each HFET was grown at the base of a GaN microcantilever. The layers comprising the HFET mesa thickness and cantilever beam thickness are labeled.

A brief fabrication procedure will now be given. The AlGaN/GaN layer structure was grown on a silicon substrate (111) with a thickness of ~675 μm. Before growing a 1 μm undoped GaN layer, a buffer layer was employed as a transition layer. The thickness of our microcantilevers is formed by this transition layer and the undoped GaN layer as shown in Fig. 3.1. To create the heterojunction, a thin layer of AlGaN was grown on top of the GaN layer. Cantilevers were outlined using typical photolithographic procedures, using masks developed in AutoCAD and ordered from Photo Sciences, Inc. Beginning at this point, there are 16 major phases of the manufacturing process, which are depicted in Fig. 3.2 [19]. Beginning with step (a), 6” wafers were diced into square pieces (1.4 cm ×
1.4 cm). Next in step (b), the SiO$_2$ is then deposited using a plasma-enhanced physical vapor deposition (PECVD) technique. In step (c), the SiO$_2$ is then photolithographically patterned and etched with an Inductively Coupled Plasma (ICP) tool. The patterned SiO$_2$ serves as a hard mask to etch the AlGaN layer and define the mesa structure (14 $\times$ 34 µm), which is the active area where AlGaN/GaN HFETs are built. In step (d), the AlGaN is etched using a dry etching recipe of GaN based on BCl$_3$/Cl$_2$. The AlGaN layer is over etched far into the GaN layer to form a distinct mesa outline. In step (e), SiO$_2$ is deposited again through PECVD and then patterned [step (f)] and etched [step (g)] to serve as a hard mask for etching GaN to define the cantilever contour. After defining the cantilever outline, SiO$_2$ is removed from the top using buffered oxide etchant (BOE) in step (h). Then, in step (i) ohmic contacts for the drain and source terminals are formed from a multilayer metal stack of Ti (20 nm)/Al (100 nm)/Ti (45 nm)/Au (55 nm), followed by rapid thermal processing (RTP) at 800 °C for 60 seconds in the presence of N$_2$. In step (j), Ni (25 nm)/Au (375 nm) is then deposited to form the Schottky contact for the gate terminal. E-beam evaporation is then used to deposit the bonding pads [step (k)], which are linked to the source/gate/drain terminals. Au was used, along with a Ti adhesive layer. The chips are flipped over [step (l)], and SiO$_2$ is deposited beneath [step (m)], which is then patterned [step (n)] to serve as a hard mask for etching Si. Finally, in step (o), the cantilevers are released by etching the Si substrate from below using a Bosch process. By alternating a 10-second SF$_6$ etch cycle with a 7-second C$_4$F$_8$ passivation cycle, Si is anisotropically etched. The specifics of fabrication difficulties and process
optimization are explored elsewhere [20]. Scanning electron microscope (SEM) images of microcantilevers with AlGaN/GaN HFETs at the base are included in Fig. 3.3 [20].

**Figure 3.2:** Representative process flow diagram for a similar piezotransistive GaN-based microcantilever [19].
Figure 3.3: (a) SEM image of 14 GaN microcantilevers. (b) SEM image of 4 microcantilevers. (c) SEM image of 1 microcantilever. (d) SEM image of an AlGaN/GaN HFET formed at the base of a GaN microcantilever. All images used from Ref [20].

3.2 Measurement Setup

To study the trapping/detrapping effects of sub-bandgap light on the HFET surface, we used 635 nm, 520 nm, and 405 nm wavelength lasers with rated powers of 125 mW, 25 mW, and 30 mW, respectively. We incorporated the fluorescent room lights (which typically emit some UV components [16, 21]) into some of our HFET response
measurements for additional comparison. A ×4 neutral density filter (NDF) was used to reduce laser intensity by 75% when appropriate.

Figure 3.4 shows a wire bonded processed chip attached to a 28-pin dual inline package (DIP) chip carrier and the HFET layout. A chip containing several cantilevers was glued to the chip carrier with the gate, drain, and source contact pads wire bonded to designated pins on the chip carrier. Figure 3.5 gives the schematic of the experimental setup used to measure changes in HFET channel resistance from laser exposure at different levels of gate bias. A laser was focused and pulsed at two different locations: Position 1, slightly in front of the HFET (with the less intense areas of the gaussian distributed beam still overlapping the HFET), and Position 2, directly on the HFET. Prior to turning on the laser, a negative voltage was applied to the gate, and a constant current was supplied from drain to source (I_DS). A precision source/measure unit (SMU, model B2912A) from Keysight Technologies was used to supply a constant current (typically 10 µA) while simultaneously measuring the drain-source voltage (V_DS). Changes in HFET channel resistance were tracked by monitoring changes in V_DS (directly proportional to changes in drain-source resistance (R_DS) as the I_DS is held constant). A lock-in amplifier (SR850, Stanford Research Systems) was used to apply the HFET gate bias and supplying the control signal for pulsing the laser (the laser was pulsed at 100 Hz for the purpose of reducing damage to the HFET from sustained exposure).
**Figure 3.4:** Close-up images of a measurement-ready device. From top to bottom in the clockwise direction: Photo of GaN microcantilevers mounted and wire bonded to a gold-coated chip carrier; Microscope image (5×) of 3 microcantilevers; Microscope image (10×) of 1 microcantilever; Microscope image (20×) of an AlGaN/GaN HFET at the base of a microcantilever.

**Figure 3.5:** Schematic view of experimental setup.
3.3 HFET Characterization

Two similar HFETs were used throughout our experiments, referred to as “Device 1” and “Device 2”. Basic electrical characteristics, i.e., $I_{DS} – V_{DS}$ and $I_{DS} – V_{GS}$ curves, for both HFETs are shown in Fig. 3.6. The device characteristics were used to calculate the 2DEG mobility in the non-saturated regime ($\mu_{2DEG}$) using the equation:

$$\mu_{2DEG} = \frac{L_{ch} g_{m}}{W_{ch} V_{DS} C'_{eff}}$$  \hspace{1cm} (3.1)

and the sheet carrier density using equation:

$$n_s = \frac{1}{q R_{sheet} \mu_{2DEG}}$$ \hspace{1cm} (3.2)

where $L_{ch}$ is channel length (11.5 $\mu$m), $W_{ch}$ is channel width (14 $\mu$m), $C'_{eff}$ is the effective capacitance per unit area between the gate and the channel, $R_{sheet}$ is channel sheet resistance, $q$ is elementary electron charge, and $V_{DS}$ is the drain-source voltage, which was kept at 0.5 V to correspond to the value of transconductance ($g_m$) obtained from the $I_{DS} – V_{GS}$ measurements. The value of $R_{sheet}$ was calculated as $R_{sheet} = R_{DS} \frac{W_{ch}}{L_{ch}}$, with $R_{DS}$ being the drain-source resistance under zero gate bias (measured in the dark as 861.15 $\Omega$). The Device 1 sheet resistance calculated from the above formula was found to be 1048.4 $\Omega/\square$. The effective capacitance $C'_{eff}$ considering both the 3 nm
GaN cap layer and the 20 nm AlGaN barrier layer, is given as

\[ C'_{\text{eff}} = \left( \frac{1}{C'_{\text{GaN}}} + \frac{1}{C'_{\text{AlGaN}}} \right)^{-1} \]

with capacitance per unit area of the respective layers given as

\[ C'_{\text{GaN}} = \frac{\varepsilon_0 \varepsilon_{\text{GaN}}}{t_{\text{GaN}}} \quad \text{and} \quad C'_{\text{AlGaN}} = \frac{\varepsilon_0 \varepsilon_{\text{AlGaN}}}{t_{\text{AlGaN}}} \]

where \( t_{\text{GaN}} \) and \( t_{\text{AlGaN}} \) are the GaN cap layer and AlGaN barrier layer thicknesses. Furthermore, \( \varepsilon_{\text{GaN}} \) and \( \varepsilon_{\text{AlGaN}} \) are the GaN and AlGaN dielectric constants, and \( \varepsilon_0 \) is vacuum permittivity. For 25% Al composition, \( \varepsilon_{\text{AlGaN}} \) was computed as 9.375 [2], and the \( C'_{\text{eff}} \) was calculated from the above formula as 361.52 nF/cm².

Figure 3.6(a) gives the \( I_{DS} - V_{DS} \) characteristics for Device 1, where \( V_{GS} \) was decreased from 0 V down to -4.2 V in steps of -0.1 V. The maximum saturation drain-source current (\( I_{DSS} \)) was found (from the \( V_{GS} = 0 \) V curve) to be 2.97 mA, which reduced monotonically and very uniformly with application of more negative gate bias. Figure 3.6(b) shows an \( I_{DS} - V_{GS} \) curve for Device 1 with \( V_{DS} \) set at 0.5 V, from which the threshold voltage (\( V_T \), arbitrarily defined as the value of \( V_{GS} \) where the \( I_{DS} \) is 1000 times smaller than \( I_{DSS} \)) was determined to be \( \sim -3.82 \) V. The transconductance \( g_m \) was obtained to be 287.6 \( \mu \)S, from the slope of the linear region of the curve [shown by the black dotted line in Fig. 3.6(b)]. Using this value of \( g_m \), along with the values of \( C'_{\text{eff}}, V_{DS}, L_{ch}, \) and \( W_{ch} \), the \( \mu_{2\text{DEG}} \) was found from Eq. (3.1) as 1307 cm²/V-s, which agrees with previously reported values (\( > 1000 \) cm²/V-s [3]). The \( n_s \) was calculated from Eq. (3.2) as \( 4.56 \times 10^{12} \) cm², which is lower than typically expected from theoretical considerations (\( \sim 10^{13} \) cm² [2]), likely due to high density of trapped electrons from extensive usage/biasing of the device, but comparable to previously reported values for these devices [22]. Using the same methods as above, \( \mu_{2\text{DEG}} \) and \( n_s \) values for Device 2
were extracted from I-V measurements, which are shown in Figs. 3.6 (c) and (d). From the $I_{DS} - V_{DS}$ curves in Fig. 3.6(c), we obtained $I_{DSS} = 2.63$ mA, and $R_{DS} = 1153.69$ Ω. From Fig. 3.6(d), we found $g_m = 218 \, \mu\text{S}$ and $V_T = -3.93$ V. Using these values in Eq.’s (3.1) and (3.2), we obtained the mobility and carrier density as $\mu_{2DEG} = 990.7 \, \text{cm}^2/\text{V-s}$ and $n_s = 4.49 \times 10^{12} \, \text{cm}^{-2}$, respectively. We find that the 2DEG density for Device 2 is very comparable to that of Device 1, while the carrier mobility is significantly lower, which can be attributed to material and device fabrication related non-uniformities.

**Figure 3.6:** Measurements of $I_{DS}-V_{DS}$ and $I_{DS}-V_{GS}$ taken from Devices 1 and 2 in dark conditions. (a) $I_{DS}-V_{DS}$ measurements from Device 1. $V_{GS}$ was decreased from 0 V down to -4.2 V in increments of -0.1 V. (b) $I_{DS}-V_{GS}$ measurement from Device 1 with $V_{DS}$ set to 0.5 V. (c) $I_{DS}-V_{DS}$ measurements from Device 2. (d) $I_{DS}-V_{GS}$ measurement from Device 2.
3.4 Chapter 3 References


CHAPTER 4

INVESTIGATION OF SUB-BANDGAP ILLUMINATION EFFECTS ON SURFACE STATES

In this chapter, the influence of sub-bandgap illumination on the dynamics of surface trapping and detrapping will be demonstrated. We will first re-establish the effects of surface electron trapping on channel resistance without the use of a laser, depicted by measurements of V_{DS} response at different levels of applied gate bias under dark conditions. Then the effects of laser illumination on the surface will be demonstrated and discussed, first with 635 nm exposure at different levels of gate bias, while also exposed to ambient fluorescent lighting. This will be compared with 635 nm laser exposure in dark conditions. Next, the effects of laser wavelength and intensity variation on the surface will be demonstrated. Then, a physical model with band diagrams will be presented to explain our observations. Lastly, photo-assisted switching operations will be shown, employing different wavelength lasers to trap and detrap electrons from the surface.

4.1 Demonstrated Effects from Surface Trapping of Gate-Ejected Electrons

As mentioned in previous chapters, under the influence of a negative gate bias and a positive drain bias, electrons can tunnel from the gate Schottky metal contact into the
surface trap states between the gate and drain. At more negative gate bias values, the
probability of field-emission becomes greater, leading to a higher rate of electron
trapping on the surface. These trapped electrons then reduce the 2DEG density at the
AlGaN/GaN interface, which increases $R_{DS}$. Since we maintained the drain current at a
constant value of 10 µA, $V_{DS}$ increases proportionally. $V_{DS}$ measurements from Device 1
under dark conditions are shown in Fig. 4.1, which can be seen to increase in steps
corresponding to the different levels of $V_{GS}$ applied (starting from 0 V and systematically
decreasing to -3.3 V). We note that immediately following the sharp jumps due to $V_{GS}$
change are sloped rises, which can be attributed to the gradual trapping of electrons
ejected from the gate. As the $V_{GS}$ magnitude was increased the trapping rate also
increased, causing the $V_{DS}$ to rise faster, which is quite dramatic around $V_{GS} = -3.3$ V.
The sharp decline in $V_{DS}$ at the end of the final step ($V_{GS} = -3.3$ V) was caused
intentionally by setting $V_{GS}$ back to 0 V. Application of further negative gate bias would
lead to a sharper increase in $V_{DS}$, ultimately leading to a runaway condition and
saturation of $V_{DS}$ at the SMU compliance voltage (set at 10 V to protect the HFET). This
runaway condition will be discussed in detail later.

The inset of Fig. 4.1 shows the changes in $R_{DS}$ and $n_s$ from their initial, zero bias
levels. $\Delta R_{DS}(t)$ has been plotted simply by dividing the $V_{DS}(t)$ measurement data by $I_{DS}$
(constant at 10 µA) to obtain $R_{DS}(t)$, and then downshifting by the initial $R_{DS}$ value
$[\Delta R_{DS}(t) = R_{DS}(t) - R_{DS}(t = 0)]$. $\Delta n_s(t)$ is plotted next by substituting $R_{DS}(t)$ into Eq.
(3.2) to find $n_s(t)$ (using 1306.9 cm²/V-s for mobility), and then downshifting by the
initial $n_s$ value $[\Delta n_s(t) = n_s(t) - n_s(t = 0)]$. From the plot, we can see the total
increase in $V_{DS}$ is $\sim 0.24 \text{ V}$ with $R_{DS}$ increasing proportionally by 24 kΩ and $n_s$ decreasing by $3.12 \times 10^{12} \text{ cm}^{-2}$. By the condition of charge neutrality, the magnitude of $\Delta n_s$ must equal the change in trapped surface charge. So, with $n_s$ decreasing by $3.12 \times 10^{12} \text{ cm}^{-2}$, we can conclude that the density of trapped surface charge also increased by the same amount.

**Figure 4.1**: Measurement of $V_{DS}$ from Device 1 at six levels of gate bias ($-2.8 \text{ V} \leq V_{GS} \leq -3.3 \text{ V}$) in dark conditions. The sharp rises are caused by increasing the negative bias to the gate. The gradual increases which follow are due to the gradual accumulation of trapped electrons on the GaN cap layer surface near the gate. The inset shows the total changes in $R_{DS}$ and $n_s$ at each bias level.
4.2 Photon-Enhanced Electron Ejection, Surface Trapping and Detrapping

While the surface electron trapping behavior under high gate-drain electric field has been widely reported in the literature (refer to Chapter 2.4), there are only a few studies investigating the enhancement of this trapping behavior under sub-bandgap light (laser) exposure. Our investigation on this began with an accidental discovery while sweeping the focus of a 635 nm laser beam across the surface of the gold coated chip carrier (passing very briefly across Position 1, labeled in Fig. 3.5), which resulted in a significant spike in $V_{DS}$. Further exploring the cause of the spike, we held the laser location constant in Position 1 and recorded the $V_{DS}$ responses at six different levels of $V_{GS}$ (varying from -2.6 V to -3.35 V). The laser was turned on after each gate bias adjustment, resulting in the transients shown in Fig. 4.2, which are plotted against a $V_{DS}$ measurement obtained without laser exposure under the same biasing conditions. Figure 4.2(a) shows the first three bias levels ($V_{GS} = -2.6\ \text{V}, -2.8\ \text{V}, -3\ \text{V}$), with arrows labeling the points where $V_{GS}$ was adjusted, and the 635 nm laser was turned on/off. As indicated in Fig. 4.2, noticeable jumps in $V_{DS}$ were observed from Device 1 under laser exposure, with the magnitude of the jumps monotonically increasing with the magnitude of gate bias. Turning the laser off caused $V_{DS}$ to reduce gradually back to its initial step level. Figure 4.2(b) gives the $V_{DS}$ measurement with more negative gate voltages, where we see more pronounced laser-induced transient behavior corresponding to more negative bias levels ($V_{GS} = -3.2\ \text{V}, -3.3\ \text{V}, -3.35\ \text{V}$). For $V_{GS} = -3.3\ \text{V}$ and -3.35 V, we find that the $V_{DS}$ increases dramatically under initial laser exposure, but also showed a strong transient reduction while the laser was still on. This transient reduction behavior is also present in
the responses at lower step levels but is much less pronounced. The inset of Fig. 4.2(b) shows $V_{DS}$ plotted in log scale, which shows that for $V_{GS} = -3.35$ V, $V_{DS}$ briefly reached the SMU compliance level of 10 V before decaying.

It should be noted that the fluorescent room lights were intentionally left on while collecting both data sets shown in Fig. 4.2, in order to facilitate a clear comparison between the laser on/off cases. The room lights provided the benefit of stabilizing the $V_{DS}$ responses beyond each gate bias induced jump, giving us noticeably flatter looking steps compared to Fig. 4.1 (especially under higher $V_{GS}$ magnitudes). Additionally, at each point where the laser was turned off, the room lights quickly reset $V_{DS}$ back to the initial step level, which allowed for a smooth transition into the next gate bias induced jump. The ambient lighting effects can be attributed to the presence of a small component of UVA (315 – 400 nm) and UVB (280 – 315 nm) radiation emitted from the fluorescent bulbs [1, 2]. These UV components being comparable to or larger than the bandgaps of GaN and Al$_{0.25}$Ga$_{0.75}$N (365 nm and 302 nm, respectively [3]), can generate electron-hole pairs within the AlGaN and GaN layers. The photogenerated electron-hole pairs are then swept by the built-in electric field across the AlGaN barrier layer, with the electrons moving to the channel to enhance the 2DEG density, and the holes moving to the surface to neutralize the trapped charges. So, the reason for the relative flatness of the blue steps in Fig. 4.2 is that a point of equilibrium was reached between the rate of surface trapping due to gate bias and the rate of electron-hole pair generation due to fluorescent room light exposure. In contrast, Fig. 4.1 measurements were taken in complete darkness, and as a result we see sloped rises in $V_{DS}$ caused by the gradual accumulation of trapped surface
charge near the gate, as mentioned previously. With the device kept completely in the dark, there was no substantial means by which the rate of surface trapping could be mitigated, so when $V_{GS}$ was adjusted to higher magnitudes, the trapping rate kept increasing monotonically with time.

The sharp initial increases in $V_{DS}$ upon exposure to the laser (more prominent for larger negative gate biases) can be attributed to significant enhancement in electron emission from the gate, and consequently higher electron trapping at the surface states, as mentioned above. However, with very similar photon flux on both the gate edge and the bare surface (almost equally covered by the large beam diameter of the laser), higher levels of surface state trapping can also lead to higher levels of emission of trapped electrons from surface states. Thus, the transient reduction in $V_{DS}$ following the initial steep rise is likely caused by laser assisted detrapping of electrons from the filled surface states. This phenomenon of electron photoemission from traps has been widely studied and reported [4 – 6]. After the high rate of electron injection into the surface states (indicated by the initial jump in $V_{DS}$), the detrapping rate increases considerably, which then gradually decreases until equilibrium is reached between the two rates. This is exhibited by the monotonically reducing $V_{DS}$ transient following the spike, which eventually levels out.
Figure 4.2: Measurement of Device 1 VDS response from 635 nm laser exposure (shown in red) plotted against a measurement of VDS without the laser (shown in blue) at six levels of gate bias (-2.6 V ≤ VGS ≤ -3.35 V). The HFET was exposed to fluorescent room lighting for the duration of both measurements. (a) Zoomed-in view of VDS responses at the first three bias levels (-2.6 V, -2.8 V, -3 V). The transient at a single VGS level is labeled, with arrows indicating the point where VGS was adjusted, and where the 635 nm laser was switched on/off. (b) Full view of VDS transients observed across the entire range of VGS. The inset shows the same plot in log scale, with the peak value visible at VGS = -3.35 V.
In contrast to the above, we also studied the trapping dynamics with the room lights off and the results are shown in Fig. 4.3. These measurements were taken using Device 2. We found that with the application of a negative gate voltage (-3.3 V) the initial quick rise in $V_{DS}$ is observed, followed by a relatively flat region, which is then followed by a sloped increasing transient. When the red laser is turned on, there is a sharp rise in $V_{DS}$, caused by the photoemitted electrons from the gate getting trapped at the surface, which stabilizes due to eventual equilibrium between the trapping and detrapping rates, as observed in Fig. 4.2. However, as the red laser is switched off, unlike in Fig. 4.2, where the $V_{DS}$ started reducing, we observed it to increase monotonically, indicating further trapping at the surface, which was unmitigated due to the absence of the ambient room light. Finally, when the ambient light is turned on, $V_{DS}$ reduces rather sharply to the initial level, clearly underlining the role of ambient light in stabilizing the carrier dynamics in AlGaN/GaN HFETs. We would like to emphasize here that in the absence of ambient lighting, the laser itself can stabilize $V_{DS}$, after the initial jump, as indicated by the stable $V_{DS}$ reached under prolonged laser exposure. This indication of equilibrium between the rates of trapping and detrapping further establishes the role of the laser in facilitating both mechanisms simultaneously. Further discussion on these trapping/detrapping dynamics will be presented in our physical model.
Figure 4.3: Measurement of Device 2 $V_{DS}$ response from 635 nm laser exposure with the room lights off. Notable increases in $V_{DS}$ caused by gate bias adjustment, switching on the laser, and switching off the laser are all labeled. The additional rise from switching off the laser is due to thermal runaway. Also labeled is the sharp decline in $V_{DS}$, observed after turning on the room lights.

4.3 Laser Position and Wavelength Dependence on Trapping and Detrapping

We mentioned earlier that the laser position has a critical role in the trapping and detrapping rates as it influences electron injection from the gate and detrapping from the surface states. In addition, we have also observed a strong dependence of the electron trapping and detrapping dynamics on the laser wavelength and the initial gate bias stress time (which leads to different degrees of surface trapped charges at the instant of laser exposure). To further investigate these effects, we recorded sets of $V_{DS}$ transients from Device 2, changing the position of the laser between Position 1 and Position 2 (see Fig.
3.5 for the two laser positions) between measurements. We performed the studies with both the 635 nm and 520 nm lasers in absence of ambient lighting. Two sets of these position/wavelength comparisons were recorded, one for each pre-illumination gate bias stress time of 200 s and 800 s. Figure 4.4(a) compares the first set of $V_{DS}$ transients from the 635 nm and 520 nm lasers, which were turned on after 200 seconds of gate bias stress. In Position 1 (further from the HFET), before illumination from the 635 nm laser, an increase in $V_{DS}$ transient is observed as usual. When the laser is switched on there is an immediate jump in $V_{DS}$ as observed earlier (Figs. 4.1, 4.2 and 4.3), but unlike in Figs. 4.2 and 4.3 no equilibrium $V_{DS}$ state is reached, instead we see a gradually increasing $V_{DS}$ after the initial jump. However, in Position 2, with 635 nm exposure, the initial quick rise abruptly stopped short of its Position 1 peak, and was followed by a strong transient reduction in $V_{DS}$, similar to that in Fig. 4.2(a) (red curves). For the 520 nm laser exposure, the response for Position 1 was similar to that of the 635 nm laser, although the magnitude and rate of increase were significantly lower. In Position 2, the $V_{DS}$ decreased in contrast to the 635 nm exposure, and eventually reached equilibrium, remaining constant at its reduced level.

When the initial gate bias application time was increased from 200 s to 800 s, keeping the magnitude same as -3.3 V, the responses changed significantly. While the response for 635 nm laser exposure in Position 1 remained mostly similar as before (although a flat $V_{DS}$ region is observed unlike before), the response at Position 2 was different, involving a quick upward transient followed by a much more pronounced decay transient for $V_{DS}$ compared to that in Fig. 4.4(a), which caused the final $V_{DS}$ value to
reduce below the level when the laser was switched on. The responses for the 520 nm laser were also significantly different, with both position 1 and 2 exposure resulting in clear reduction in $V_{DS}$, unlike in Fig. 4.4(a), which indicated a higher rate of detrapping compared to trapping between Positions 2 and 1.

Figure 4.4: Comparison of Device 2 $V_{DS}$ responses from exposure to different laser wavelengths (635 nm, 520 nm) and relative intensities (Position 1, Position 2). Positions 1 and 2 were respectively used to demonstrate the effects of lower and higher relative intensities. Between (a) and (b), $V_{GS}$ was held for different durations before switching on the laser, in order to observe the effect of different surface charge densities prior to laser exposure. (a) Wavelength and intensity comparisons performed after 200 seconds of maintained $V_{GS}$. For visual clarity, measurements are staggered 50 seconds apart. (b) Wavelength and intensity comparisons performed after 800 seconds of maintained $V_{GS}$. For visual clarity, measurements are staggered 50 seconds apart (in reverse order). The inset shows a more straightforward intensity comparison, using an ×4 NDF to periodically attenuate the 520 nm laser held in Position 2 ($V_{GS} = -3.5$ V).
We would like to mention here that using a filter to reduce the optical intensity, at a given location, did affect the $V_{DS}$ value as expected. The inset of Fig. 4.4(b) shows the $V_{DS}$ response as 520 nm illumination was reduced in intensity by ~75% using a neutral density filter. When the filter was placed between the laser and HFET, $V_{DS}$ increased as expected, since the reduced intensity should reduce the detrapping process relative to the trapping process. The trapping and detrapping processes, as facilitated by laser illumination, are explained with the help of band diagrams and surface trap models in the following section.

4.4 Physical Model

To explain the observed $V_{DS}$ transients, we propose a physical model to explain the influence of sub-bandgap optical illumination on the charge trapping and detrapping effects in the HFET. Figure 4.5(a) shows the trapping of electrons under the application of a negative gate bias and sub-bandgap illumination. Under negative bias, the primary mechanism that the electrons eject from the gate is through thermionic-field emission through the thin forbidden gap as shown in Fig. 4.5(a) [7]. These charges get trapped at the interband states at the surface or subsurface region and deplete the 2DEG density at the AlGaN/GaN interface [see Fig. 4.5(b)], which then increases the $V_{DS}$ due to the constant current condition of our setup. Under optical illumination, the electrons can also emit over the barrier to reach the surface states via internal photoemission; 635 nm and 520 nm correspond to photon energies of 1.95 eV and 2.38 eV, respectively, which are much larger than the typical gate Schottky-barrier height of 1.4 – 1.6 eV. Both these
mechanisms are shown schematically in Fig. 4.5(a). At larger negative gate bias, the reverse bias current increases, and more trapping happens near the edge of the gate, which results in more pronounced transients (both with and without laser exposure) as seen in Figs. 4.1 and 4.2. The trapped charge density can reach sufficient levels to almost completely deplete the 2DEG, increasing the drain-source resistance and the $V_{DS}$ to very high levels [Fig. 4.2(b) inset]. We believe the mechanism of thermionic-field emission is made even more pronounced, than typically observed, due to our device biasing setup, which keeps $I_{DS}$ constant while trapped electrons deplete the 2DEG. Because of this constant current condition, as $R_{DS}$ increases with trapped charge density, so does Joule heating ($I^2R$ loss) in the depleted channel region. The associated temperature rise can cause increased thermionic-field emission in a reverse biased Schottky barrier, which would cause more electron trapping, depleting the channel further, further increasing $I^2R$ heat emission, and so on. This is the thermal runaway condition mentioned earlier, which is possible if the HFET is kept in the dark under sufficient bias stress. We see the beginning of this condition in Figs. 4.1 and 4.3 with the upward sloped transients after the application of the gate bias. With enough time allowed under sufficiently high gate bias, we’ve observed these sloped transients gradually become exponential, eventually reaching the 10 V SMU compliance. Figure 4.2 shows this behavior suppressed by the fluorescent ambient lighting, as indicated by the decay in $V_{DS}$ after the laser is turned off. Even more notable however, is that Fig.’s 4.3 and 4.4 demonstrate that sub-bandgap laser exposure can also suppress this behavior.
**Figure 4.5:** (a) Band diagram illustration of the electron trapping process at the GaN cap layer surface: Electrons from the gate are emitted over/through the reverse-biased Schottky barrier into the conduction band of the exposed top layer (via internal photoemission or thermionic-field emission) and are subsequently captured by interband surface states. (b) A high density of negative charge accumulates at the surface near the gate and depletes 2DEG electrons. (c) Band diagram illustration of the electron detrapping process at the GaN cap layer surface: Sub-bandgap photons excite electrons from surface trap states into the conduction band.
The optical illumination can also enhance the opposing mechanism, by helping with the emission of the trapped charges from the surface/subsurface states. This is shown schematically in Fig. 4.5(c). Due to the large beam diameters of our lasers, it is very likely that the processes depicted in Fig’s 4.5(a) and (c) occur simultaneously at variable rates. This is also supported by our data, most notably, by the flatness in $V_{DS}$ established in Fig. 4.3 for the duration of laser exposure (after the initial rise). This flatness from Fig. 4.3 is especially significant because it occurred under dark conditions, making the laser assisted detrapping the only mechanism opposing the trapping process. Also noticeable is that after the laser was turned off, $V_{DS}$ resumed its upward trend in Fig. 4.3, an indication of increased trapping. The flatness indicates that an equilibrium condition is established shortly after the initial high rate of injection from the gate, upon turning on the laser, as indicated by the spike in $V_{DS}$. As more electrons populate the surface very close to the gate, a negative space charge region is formed, which opposes emission of gate electrons, reducing the rate of trapping. At the same time, with more electrons populating the surface, the rate of electron emission from the surface increases. Equilibrium is established when the negative space charge develops sufficiently, such that the gate electron emission rate (and subsequent trapping rate) is reduced to match the detrapping rate. The critical density of trapped surface charge constituting the negative space charge region, determines the net increase observed in $V_{DS}$, which remains constant (with an even flow of electrons entering and leaving the surface) so long as the laser intensity, focal location, and level of gate bias are maintained.
It should be noted that both laser intensity and the density of electrons in the region of laser focus are important factors in controlling the electron dynamics (ejection from gate or from trap states). This is illustrated by the responses seen with the filter being on and off [Fig. 4.4(b) inset]. Additionally, and more subtly, this is exhibited by the locational dependence of the trapping and detrapping processes observed in Fig. 4.4. While the laser is focused on the HFET (Position 2), the gate edge and HFET surface both receive the maximum intensity of the laser light, which maximizes both the electron ejection from the gate, and from surface states. When the laser is focused somewhat away from the HFET (Position 1), the intensity is reduced and the ejection rate from both the gate and surface states reduces. Ultimately what determines the accumulated density of surface charge resulting from laser illumination is how the initial ejection rate from the gate compares with that from traps. The Fig. 4.4 data suggests that the latter is affected more considerably than the former, when laser intensity is changed. Taking the Fig. 4.4(a) 635 nm transients for example, one can notice that the increase in VDS from illumination in Position 1 is higher than from Position 2. This means that in spite of the laser intensity being reduced (in Position 1), the initial net injection of carriers on the surface is greater. A reasonable explanation for this would be that the electron ejection rate from surface states has reduced more than from the gate, between Positions 2 and 1, which is likely because of the much higher density of electrons in the gate metal compared to the surface.

On the other hand, if there is sufficient density of trapped carriers already present on the surface due to prolonged bias stress, it is possible that their emission can be
facilitated at a higher rate than that from the gate. This is because the emission from the traps is strongly dependent on the magnitude of the trapped carrier density. The higher the magnitude of the trapped carrier density, the higher is the probability of electron emission upon exposure to light. In addition, the trapped electrons oppose further ejection of electrons from the gate, reducing the trapping rate. This is clearly demonstrated in the responses to 520 nm and 635 nm exposure after 200 s and 800 s of charge trapping (enabled by negative gate bias), as seen from Fig. 4.4. The higher levels of trapped charges, after 800 s of gate biasing, for both wavelengths, resulted in transient reductions of $V_{DS}$ after the initial sharp rise, and then approached equilibrium much quicker than the Fig. 4.4(a) transients. This behavior was especially noticeable under 520 nm illumination.

The difference between the responses corresponding to the 635 and 520 nm seen in Fig. 4.4 is likely due to the energy levels of the surface traps. While they both are able to get electrons to eject from the gate similarly (as their photon energies are much higher than the gate Schottky barrier), they will impact the trapped charge emission differently due to the different energy depth distribution of the surface/subsurface traps. This is shown schematically in Fig. 4.5(c), where only shallower traps emit electrons upon 635 nm laser exposure, while both shallower and deeper traps can emit upon 520 nm laser exposure, as observed experimentally in Fig. 4.4. Thus, 520 nm exposure results in a higher rate of photo-assisted detrapping, resulting in a lower equilibrium $V_{DS}$ compared to 635 nm exposure. The deepest traps can respond to 405 nm laser exposure which can also create electron-hole pairs (EHPs) due to its photon energy (3.06 eV) being quite close to the bandgap of GaN (3.42 eV), Additionally, it can result in absorption due to band tailing
and creation of photogenerated holes that can reach the surface and neutralize the trapped electrons. Thus, this laser was observed to always result in lowering of $V_{DS}$ very quickly, showing relatively little position dependence.

### 4.5 Photo-Assisted Switching Operations

Taking advantage of the resetting capability (through removal of trapped charges) of the 520 and 405 nm lasers, we exposed the HFET to sequences of 635/405 nm illumination and 635/520 nm illumination to demonstrate the possibility of photo-assisted switching ("memory") operations. As indicated by Fig’s 4.6(a) and (b), each reduction in $V_{DS}$ was caused by simultaneously deactivating our “set” laser (635 nm) and activating our “reset” laser (520/405 nm), while each following rise was caused by the opposite. For the first switching sequence shown in Fig. 4.6(a), the 635 nm laser was focused on the HFET (Position 2), while the 405 nm laser was focused on Position 1 with the gate voltage maintained at -3.45 V. While exposure to the 635 nm laser increased $V_{DS}$ through enhancement of electron trapping, exhibited by a sharp jump followed by a rising $V_{DS}$ transient, subsequent exposure to the 405 nm laser reset $V_{DS}$ almost completely. As shown in Fig. 4.6(b), we ran this sequence again, this time using the 520 nm laser to "reset". To optimize detrapping performance, the 520 nm laser was focused directly on the HFET. Both the 635/405 nm and 635/520 nm combinations resulted in quite uniform rise and fall magnitudes over multiple cycles indicating stable device operation. We note that the “reset” ($V_{DS}$ magnitude reduction) caused by the 405 nm is slightly larger than that caused by the 520 nm laser, which is expected since the creation of electron-hole
pairs by the former can lead to more efficient reduction of surface traps through recombination with holes. Looking at one individual pulse, the rise time constant for “setting” was determined to be \( \sim 1-2 \) seconds, while the fall time constant for “resetting” was found to be \( \sim 200 \) ms. Although the switching power (and time constants) required for “memory” operations in these devices are far from those necessary for practical applications, miniaturization of the devices and periodic reading (rather than continuous reading by passing constant drain current) of the high/low states could significantly reduce the operational power requirement.

Figure 4.6: \( V_{DS} \) plots demonstrating photo-assisted switching operations. Points of gate bias application and laser on/off transitions are labeled. (a) The 635 nm laser held in Position 2 is used to accumulate negative surface charge, setting \( V_{DS} \) high. The 405 nm laser held in Position 1 is used to deplete negative surface charge, resetting \( V_{DS} \) low. (b) The 635 nm laser held in Position 2 is used to accumulate negative surface charge, setting \( V_{DS} \) high. The 520 nm laser, also held in Position 2, is used to deplete negative surface charge, resetting \( V_{DS} \) low.
4.6 Chapter 4 References


CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

We have demonstrated the strong influence of sub-bandgap laser illumination on the trapping and detrapping dynamics in AlGaN/GaN HFETs. Furthermore, we have presented a physical model for this behavior, which carefully considers the effects of laser intensity variation, different wavelengths, and prolonged bias stress. This model assumes both the gate metal and the surface are concurrently subjected to equal intensity sub-bandgap light. In summary, we first established from our initial $V_{DS}$ transients that 635 nm laser exposure can induce a net increase in surface carrier density. Under dark conditions, we deduced that the very same laser was also maintaining an equilibrium level of surface charge. And for that to be possible, surface trapping and detrapping must occur at even rates. However, the initial rise in $V_{DS}$ induced by 635 nm illumination would suggest that initially, the rate of gate electron ejection and subsequent surface trapping, was greater than the rate of detrapping. Thus, there must be some mechanism by which the rates are made equal. Our proposed model suggests that a negative space charge region formed near the gate assists in establishing the equilibrium condition.

Exploring the effects of intensity variation, we found that reduced intensity of incident 635 and 520 nm light on the HFET favored electron emission from the gate, over emission from surface traps. This behavior was likely due to the higher density of electrons in the gate metal compared to the surface. The trapping/detrapping activity was
also found to be a strong function of laser wavelength with the 635 nm laser facilitating relatively high rates of trapping, while comparatively, the 520 nm laser seemed to favor the detrapping process more. A sub-bandgap 405 nm laser, with photon energy closer to the GaN bandgap, was observed to produce an overwhelming detrapping response that can be attributed to the annihilation of trapped electrons by photogenerated holes. The carrier dynamics were also found to be dependent on the density of trapped surface charge as well, which was a function of the duration of negative gate bias prior to illumination. Lastly, applying this phenomenon of trapping and de-trapping assisted by sub-bandgap photons, red, green, and purple lasers were used to demonstrate photo-assisted dynamic switching operations by manipulation of surface-trapped carriers.

5.2 Direction of Future Research

One of the main issues we encountered was the inability to keep power density constant between our three lasers. The laser spot sizes, and power ratings were all different from each other. For this reason, we needed to generalize our claims regarding the wavelength comparison results. While theory certainly supports our observations, the differences in V_DS behavior between lasers cannot be purely attributed to the differences in wavelength. In the future, it would be interesting to perform these experiments again with several power matched lasers of different wavelengths, or perhaps just one laser with a tunable wavelength feature. Tunable laser power output would also be desirable for better V_DS comparisons between various laser intensities. If constant power and beam
diameter can be assured across different wavelengths, we can better validate our results from this work.

Another issue we encountered was the beam diameters of our lasers, which covered the entire HFET, and then some. If we could reduce the diameter to target either the surface or the gate, without any overlap, we could observe the trapping/detrapping responses individually, instead of lumping them both together in a single measurement.

Additionally, it would be interesting to see how these demonstrated effects might differ if we had passivated the surface (with SiNx, AlN, or SiO2). I expect that we might observe the same type of trapping/detrapping behavior, but much less pronounced due to the lower density of traps. It might also be reasonable to expect the equilibrium of the observed behavior to favor detrapping more than trapping. With fewer traps due to surface passivation, the initial density of electrons injected from the gate into traps should be much less. So, it seems possible that sub-bandgap exposure would mostly serve to emit electrons from traps. This appears to be what was reported by Kang et al. [1, 2], but would still be interesting to see for ourselves.

Lastly, something that we began to investigate, but were not able to complete, is the effect of coating the surface with metal nanoparticles (NPs) on this trapping/detrapping behavior. We had used NP coatings several times on our microcantilevers to enhance absorbed photon energy and strengthen the generated photoacoustic waves through the material. This was reported earlier by our group to enhance the resonance amplitude (ΔVDS) measured from the HFET at the base of the cantilever [3]. From measurements of HFET illumination response, the only trend that we
were able to observe was that the gate bias at which thermal runaway occurred (from laser exposure) seemed to be lower for our Au, Ag, and Pd coated devices compared to the uncoated ones. But there is no direct proof of causation here, and we never actually compared $V_{DS}$ responses from one device, before and after NP deposition. This is something I would like to try in the future.

5.3 Chapter 5 References

