A Hybrid Method of Performing Electric Power System Fault Ride-Through Evaluations on Medium Voltage Multi-Megawatt Devices

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A HYBRID METHOD OF PERFORMING ELECTRIC POWER
SYSTEM FAULT RIDE-THROUGH EVALUATIONS ON
MEDIUM VOLTAGE MULTI-MEGAWATT DEVICES

A Dissertation
Presented to
the Graduate School of
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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy
Electrical Engineering

by
John Curtiss Fox
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Accepted by:
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ABSTRACT

This dissertation explores the design and analysis of a Hybrid Method of performing electrical power system fault ride-through evaluations on multi-megawatt, medium voltage power conversion equipment. Fault ride-through evaluations on such equipment are needed in order to verify and validate full scale designs prior to being implemented in the field. Ultimately, these evaluations will help in reducing the deployment risks associated with bringing new technologies into the marketplace. This is especially true for renewable energy and utility scale energy storage systems, where a significant amount of attention in recent years has focused on their ever increasing role in power system security and stability.

The Hybrid Method couples two existing technologies together – a reactive voltage divider network and a power electronic variable voltage source – in order to overcome the inherent limitation of both methods, namely the short circuit duty required for implementation. This work provides the background of this limitation with respect to the existing technologies and demonstrates that the Hybrid Method can minimize the fault duty required for fault evaluations. The physical system, control objectives, and operation cycle of the Hybrid Method are analyzed with respect to the overall objective of reducing the fault duty of the system. A vector controller is designed to incorporate the time variant nature of the Hybrid Method operation cycle, limit the fault current seen by the power electronic variable voltage source, and provide regulation of the voltage at the point of common coupling with the device being evaluated.

In order to verify the operation of both the Hybrid Method physical system and vector controller, a controller hardware-in-the-loop experiment is created in order to simulate the physical system in real-time against the prototype implementation of the vector controller. The
physical system is simulated in a Real Time Digital Simulator and is controlled with the Hybrid Method vector controller implemented on a National Instruments FPGA.

In order to evaluate the complete performance of the Hybrid Method, both a synchronous generator and a doubly-fed induction generator are modeled as the device under test in the simulations of the physical system. Finally, the results of the controller hardware-in-the-loop experiments are presented which demonstrate that the Hybrid Method is a viable solution to performing fault ride-through evaluations on multi-megawatt, medium voltage power conversion equipment.
DEDICATION

To Erica

For understanding the early mornings, late nights and short weekends,

for always being reassuring and

for being the love of my life.
ACKNOWLEDGMENTS

This work would not have been possible without the love and support of my mother and father, Pat and John Fox, who have been so understanding and supportive of my education throughout the years it has taken me to reach this point.

I thank my advisor, Dr. Randy Collins, for all of the lessons, both academic and professional, he has imparted on me through my graduate studies. His wisdom, experience, and ability to turn a quick question into a two hour conversation have taught me more than I ever could have imagined.

I am very grateful to Dr. Nikolaos Rigas for taking a chance on me and letting me take part in the initial design concepts of the WT-DTF project. Without this, there probably wouldn’t have been a grid simulator project and there definitely wouldn’t have been the best Vaudeville act in Clemson history.

I thank Dr. Tom Salem for all of the work he has done with the Grid Simulator project, especially in taking over the equipment procurement process. I almost think his persistent reminders to keep my dissertation scope contained have paid off.

I greatly appreciate Dr. Mark McKinney and Ben Gislason for listening to me rant about my trials and tribulations in learning RSCAD and LabVIEW in order to complete this work. I now realize that I must have sounded like Charlie Brown’s teacher at times.
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CHAPTER ONE
INTRODUCTION

The research presented in this dissertation will focus on the interconnection dynamics of large distributed generation devices during faults. More specifically, the research focuses on a method of presenting a power system fault to multi-megawatt devices when connected to an arbitrary bus for the purposes of evaluating the fault ride-through capabilities of such devices, with an emphasis on wind turbine generators. The behavior of large devices during power system dynamic events, such as faults, is related in part to the device’s control system and other specific characteristics, and the interaction with the power system characteristics. In order to perform such an analysis of a faulted device, a highly detailed and sophisticated model of the device and the power system is required. The results, however, will be no more accurate than the model.

At present, the ability to test multi-megawatt devices and provide model verification is not readily available in a controlled laboratory environment. Thus, device model verification often occurs once the devices are deployed in the field by capturing and analyzing data acquired during power system disturbances, such as faults or by utilizing containerized field methods of inducing power system faults for testing purposes. This is a costly and undesirable means of testing and cannot begin to replicate the conditions that could exist on an arbitrary system.

A simulated grid fault system that could replicate a realistic fault, and the resulting interaction between the power system bus and the device under test, would address the problems cited above, enabling large distributed generation systems to be advanced. For example, advanced models and control systems could be developed using information gained from a simulated grid fault system. Further, such a system would further innovation by establishing
realistic grid compatibility standards of existing and future renewable energy and energy storage technologies. For example, grid connection standards designed to ensure grid compatibility tend to not address the impact that point-in-wave of the fault events has on devices, nor do they discriminate between best and worst case scenarios when evaluating devices to the standard.

It is anticipated that this research will assist in driving future domestic and international standards by providing a method that is capable of replicating power system faults with importance placed on the point-in-wave, while also building the foundation for future grid compatibility evaluations associated with frequency response of devices during a fault event. Ideally, this will result in reducing the risk associated with deploying new technologies and ultimately drive down the costs related to meeting renewable energy generation targets worldwide.

The fundamental contribution to the literature accomplished by this research involves developing a Hybrid Method of performing fault ride-through evaluations that minimizes the hardware design complexities and increases scalability while meeting or exceeding the performance characteristics of the existing technologies. The Hybrid Method incorporates the advantages of both of the existing technologies by coupling two methods together in order to produce a system that is capable of overcoming the predominant disadvantage common to both of the existing methods (i.e., the short circuit duty).

By physically coupling a reactive divider network and a power electronic-based variable voltage source together, the Hybrid Method dramatically changes the design philosophy behind either of these two methods alone. This hybrid system is required to replicate the dynamic behavior of a real power system at the common-coupling point (bus), in response to the dynamics of the device under test. Such a system is not known to exist, nor are the controls
required for such as system. This research will extend the technical understanding by providing novel approaches to system configuration, analysis, and control in order to achieve the performance objectives required to perform fault ride-through evaluations.

The research will begin with the theoretical analysis of the Hybrid Method for the purposes of developing analytical approaches to optimizing the configuration of the reactive divider network, the open-loop control variables, and the closed-loop response of the variable voltage source based upon the characteristics of the device to be evaluated. Essential considerations include compensating for the voltage drop across the series impedance, the short circuit duty seen by the variable voltage source, and the impact of system limitations on the voltage regulation.

With respect to control system design, the Hybrid Method utilizes the switched circuit of a reactive divider network, implying that the physical system of the Hybrid Method can be classified as a multiple-input, multiple-output, linear, time-variant system. However, when a voltage matching transformer is used, a nonlinear element is introduced into the physical system for which the control system must bound the system states into a region that can be approximated as a linear system. Investigations into the control strategies for the Hybrid Method have shown that a vector control system can be developed in order to constrain the system into an approximately linear region while managing the time varying nature inherent to the Hybrid Method. This investigation into limiting the nonlinear behavior of the voltage matching transformer has resulted in passive methods of transformer flux filtering given varying voltage magnitude and phase. These methods represent the enabling technology with respect to practical implementation of the Hybrid Method of performing fault ride-through evaluations.
The vector control system for the Hybrid Method deviates significantly from vector control systems found in the literature because the Hybrid Method’s physical system cannot be constrained within a vector space without a significant loss of functionality. Thus, the common practice found in the literature of constraining the physical system in order to allow for a reduced order control system is not an applicable solution. The culmination of this research results in the development of a vector control system designed to operate the Hybrid Method of performing fault ride-through evaluations.

Finally, the detailed modeling of the Hybrid Method and simulation of the vector control system is developed in order to verify and validate the functionality, controllability, accuracy, and robustness of the complete system. The simulation of the physical system will be performed in real-time and will be coupled with a prototype vector controller configured to control the simulation of the physical system in a classic controller hardware-in-the-loop application. The controller hardware-in-the-loop experiments are designed to demonstrate the feasibility of the Hybrid Method vector control algorithms with respect to actual application that incorporate a real physical system. The modeling and simulation exercise will include characteristics of two generator types (synchronous and doubly-fed) in order to demonstrate the versatility of the vector control system and evaluate any inherent limitations with respect to physical constraints placed upon the system.
CHAPTER TWO
BACKGROUND

The scalability of wind generation, into the 100’s of MW per wind park, has fundamentally changed how power system operators view grid management and respond to fault events on the power system. Early wind turbine generators were not required to contribute or even ride-through a fault event on a power system. In some scenarios, this would require system operators to scramble to find additional generating resources in order to counter the loss of generating capacity of an entire wind park. Recognizing the issue, regulatory authorities for power systems with high penetrations of wind generation have advocated for regulations to ensure that wind turbines could, at the very least, ride-through a fault event and resume generation of reactive and active power quickly once the fault was cleared from the system.

Fault Ride-Through (FRT) is defined as the ability of an electrical device connected to the power system to withstand momentary deviations of terminal voltage that vary significantly from the nominal voltage without disconnecting from the power system. Since the most likely cause for excessive voltage deviations in a power system is a fault in the system, the term “fault ride-through” is sometimes used to encompass other reduced voltage events, such as lack of instantaneous reactive power support or large cold load pickups. In contrast to reduced terminal voltage, a fault event on power systems with specific characteristics may also cause a momentary rise in voltage. Distinguishing among all of the encompassed events has led to sub-classifications within FRT: Low-Voltage-Ride-Through (LVRT), Zero-Voltage-Ride-Through (ZVRT), and High-Voltage-Ride-Through (HVRT). It is often appropriate to lump LVRT and ZVRT together as just LVRT because they differ only in the magnitude of voltage drop.
The importance of FRT capabilities in terms of grid compatibility and overall system security has led many power system regulators to set their own fault ride-through requirements for non-standard generation sources (wind, solar, etc.). These FRT requirements vary among power system regulatory authorities since the needs of each specific system can be quite diverse [1], [2], [3], [4], [5]. Figure 2.1 demonstrates the LVRT withstanding curves specified in various grid codes throughout the world [6]. These withstanding curves define only the duration of the event and the depth of the voltage and do not define any point-in-wave information associated with the initiation and clearing of the fault. While a point-in-wave specification for a symmetrical fault is somewhat nebulous, the point-in-wave becomes more important in unsymmetrical fault scenarios where the fault is isolated to one or two phases.

![Figure 2.1: The LVRT withstanding plots versus time for various grid codes throughout the world. Updated from [6] to include the latest FERC Order No. 661-A regulation [1].](image)

The initial concept of performing field testing for LVRT and ZVRT was to use a reactive voltage divider to subject the terminals of a wind turbine generator (WTG) to a simulated fault
event as in [7]. Figure 2.2(b) demonstrates the basic concept of a utility side reactive voltage divider. Series impedance is used to limit the fault current from the utility, $I_U$, and the apparent voltage at the terminals of the WTG, $V_T$, is effectively set by the ratio of the shunt impedance to the sum of the shunt and series impedances [8]. Figure 2.2(a) demonstrates the open circuit characteristic with no device connected to the point of common coupling for [7]. While this open circuit characteristic is trivial with an indicative voltage divider, in practice there are many variables that contribute to the amount of series and shunt impedance required for a specific voltage level with a device connected to the point of common coupling, including: utility short-circuit MVA, WTG generated power, and WTG design type.

![Diagram](image)

Figure 2.2: (a) The tolerance of voltage drop from IEC 61400-21 [7] and (b) the basic reactive divider concept for LVRT/ZVRT field testing outlined in IEC 61400-21

The present methodologies for testing wind turbines against LVRT/ZVRT withstanding curves includes testing multiple rectangular voltage drops for varying duration in order to ensure that the WTG does not inadvertently trip. In [9], actual field testing with this methodology has been implemented to meet the specific requirements of a grid code’s fault ride-through withstanding curve through successive rectangular voltage dips. While this may prove to provide sufficient evidence for ride-through capabilities, a rectangular voltage dip is not always
the correct representation of a fault event and may not properly represent the voltage profile given varying system conditions or in cases of unsymmetrical system faults [10]. This is especially true given the delayed voltage recovery phenomenon that is prevalent in systems with high penetrations of line-connected induction motors [11].

To this day, efforts continue from system regulators to develop standards for fault ride-through (FRT) of renewable generation including withstanding voltage curves that define general characteristics of faults on their systems and with wind turbine manufactures by incorporating FRT capabilities into existing and future designs. While the wind energy market was the first to experience the growing pains associated with the need for FRT because of wind energy’s inherent scalability, many of the requirements and technologies developed in the process will span into other utility scale renewable energy and energy storage markets. However, with the multitude of variables involved in the problem of fault ride-through of wind turbines, these efforts have proven to be a nontrivial task for wind turbine manufacturers and end users from research, development, and operation standpoints.

The challenges associated with incorporating FRT capabilities into wind turbine generators stem from several factors, including: the diversity of wind turbine generator designs, the coupling of electrical and mechanical dynamics within the turbine drivetrain, and the ability to evaluate FRT performance in a laboratory environment where the variables can be manipulated and controlled. With the diversity of wind turbine generator designs, it is clear that the FRT technology developed for one design may not correspond directly to that of another design. The fault characteristics of a doubly fed induction generator (DFIG) with a gearbox can be very different than those of a full conversion, direct drive generator and there are numerous wind turbine design variations in between. Since the mechanical dynamics of full scale
drivetrain components do not translate into smaller scale components and are subject to high degrees of uncertainty in modeling and simulation, the coupling of electrical and mechanical dynamics in response to a fault event necessitates a need for full scale evaluation of FRT capabilities.

**Basic Fault Characteristics of Electrical Machines**

Prior to the discussion on the existing technologies for performing fault ride-through evaluations, the fault characteristics of two basic electrical machine types, synchronous and induction machines, is presented to formulate the basis of the most extreme scenarios with respect to fault ride-through evaluations. While the characteristics presented here are well established in the literature, they demonstrate characteristics of line-connected electrical machines that can be difficult to handle with any fault ride-through evaluation technology. At the root of the basic fault characteristics of these electrical machines is the fact that sharp voltage transients will result in asymmetrical components and that the initial cycles of a fault event can produce rather large fault currents compared to the nominal rating of the electrical machine.

The fault characteristics of the electrical machines demonstrated in this section are of the most simplistic form, a symmetrical three phase fault, and are not intended to be an exhaustive study of the characteristics of fault currents generated by all machine types or the characteristics given unsymmetrical fault scenarios. These simplified fault characteristics are presented to demonstrate the dynamic characteristics, not the detailed dynamic model, of machine types in order to justify the design and control of the Hybrid Method. Clearly, if the specific dynamic behavior of the machines were directly calculable or modelable, the need for fault ride-through
evaluations would not exist. Additionally, the introduction of advanced fault ride-through controls and alternative electrical machine topologies, most notably multi-megawatt wind turbine generators, greatly increases the complexity of the dynamic fault current characteristics of any given technology.

The classic fault current characteristic equation for a synchronous machine is given in Equation 2.1 [12] and an example waveform of the per unit fault currents is given in Figure 2.3 for a change in voltage equal to the rated terminal voltage. This is equivalent to zero remaining voltage at the terminals of the machine. The classic analysis of the fault current produced by a synchronous machine contains four fundamental components: an asymmetrical, sub-transient, transient, and steady-state symmetrical components. The asymmetrical component is a function of the sub-transient reactance of the machine and is subjected to the complete time constant of the machine’s parameters along with those of the external system including the fault impedance. The sub-transient and transient symmetrical components are subjected to the transient response of the machine itself. Typically, the sub-transient response is on the order of one to two cycles and the transient response can be on the order of tens of cycles before the system reaches the steady-state operating condition [13].

\[ i_F(t) = \sqrt{2}E \left( \frac{1}{X_d'} - \frac{1}{X_d} \right) e^{-\frac{t}{\tau_d}} + \frac{1}{X_d'} e^{-\frac{t}{\tau_d}} + \frac{1}{X_d} \right) \cos(\omega t) - \left( \frac{\sqrt{2}E}{X_d'} \right) e^{-\frac{t}{\tau_a}} \]  \hspace{1cm} 2.1
Figure 2.3: An example waveform for a short circuit at the terminals of a synchronous machine.

The most important factors with respect to fault ride-through evaluations is that synchronous machines exhibit high initial fault currents with asymmetrical offsets that can last for significant periods of time and that these fault currents will decay exponentially as the fault continues. The asymmetrical offsets and high instantaneous currents must be managed to ensure that the test equipment is not damaged, while at the same time the voltage at the point of common coupling must continuously be regulated by tracking the exponentially decaying fault current.

The induction machine has somewhat similar characteristics to those of the synchronous machine as demonstrated by the fault current characteristic Equation 2.2. The example waveform of the per unit fault currents is given in Figure 2.4 for a change in voltage equal to the rated voltage of the machine. In contrast to the synchronous machine, where the excitation is provided by the external excitation of the field winding, the excitation of a typical induction machine is generated from the stator flux cutting through the shorted rotor windings to produce a
counter flux and is proportional to the stator voltage. Thus, the induction machine does not exhibit transient or steady-state characteristics for a three-phase, zero-voltage fault because the fault essentially removes the excitation from the machine. However, because the flux in the rotor cannot decay instantly, the machine does exhibit sub-transient and asymmetrical fault current characteristics.

\[ i_f(t) = \left( \frac{\sqrt{2}E}{X_m} \right) e^{-\frac{t}{\tau_d}} \cos(\omega t) - \left( \frac{\sqrt{2}E}{X_m} \right) e^{-\frac{t}{\tau_s}} \]  

2.2

Figure 2.4: An example waveform for the short circuit at the terminals of an induction machine.

While the fault current characteristics for the two types of electrical machines demonstrated above do not constitute the complete behavior of more complex technologies, such as doubly fed induction generators (DFIGs) or permanent magnet full conversion machines typically employed in multi-megawatt renewable generation applications, they do illustrate the characteristics of line connected machines that should be accounted for when designing a system to perform fault ride-through evaluations. More importantly, because the DFIG type machine
has line connected stator windings, it can be extrapolated that such a machine will exhibit behavior somewhere in between that of a synchronous machine and that of an induction machine [14]. While a fair amount of literature has focused on the characterization of DFIGs and their complex controls designed for fault ride-through, the direct characterization of these machine types in industry is extremely difficult given the different design and control practices of each manufacturer [15].

**Existing Fault Ride-Through Technologies**

The present state-of-the-art for performing full scale evaluations of FRT capabilities is confined to two distinctly different technological approaches: a reactive divider network (RDN) method or a variable voltage source (VVS) method. In this document, only a very concise analysis of the advantages and limitations of each technology will be presented to provide the evidence that a third, hybrid technology, can be developed to incorporate the advantages of both existing technologies while minimizing their limiting factors. The Venn diagram in Figure 2.5 illustrates the potential advantages of such a hybrid technology. It should be noted that, presently, only field testing using a reactive divider network has actually created published results of a fault event on a multi-megawatt wind turbine.
Reactive Divider Network

The reactive divider network consists of series and shunt inductive impedances in a classic voltage divider network in which the series impedance limits the short circuit duty from the point of common coupling with the grid and the shunt impedance is switched into the circuit to initiate the fault event and switched out of the circuit to clear the fault. The shunt impedance is connected at the point of common coupling with the device under test such that the voltage seen by the device under test is the resultant of the subsequent voltage divider created by the series and shunt impedances. This method is typically employed in the field where large, short circuit duties available from the point of common coupling with the grid allow for the impedances to be relatively small in order to increase voltage regulation during the fault event. Several renewable generation manufacturers and third party compliance testing equipment manufacturers have containerized solutions for field testing [9], [16], [17] and have successfully
certified wind turbines in the field. However, this has proven to be a costly endeavor, as the test equipment must be transported to the installed location of the wind turbine and certification can require full load generation during the fault event, which is dependent upon the wind conditions in the field. That being said, some efforts have been made to bring this method into a laboratory environment where large short circuit duties are available [18]. However, to allow for testing at both 50 and 60 Hz in [18], a large motor-generator set is utilized to support the reactive divider network’s short circuit duty requirements, which requires significant capital investment for a system with very limited ancillary uses [8].

This reactive divider network method is limited in terms of controllability because the fault events are restricted to rectangular voltage profiles, the recovery voltage profile is constrained by the voltage at the point of common coupling with the grid, and the fundamental frequency is established by the grid as well [19]. The evaluation of FRT characteristics with a reactive divider network does offer a realistic fault characteristic with regards to sequential clearing of individual phase faults as the current passes through zero crossings by the employment of circuit breakers to insert and remove the shunt element. Additionally, because the reactive divider network utilizes inductive elements for the shunt impedance, the characteristics of the fault represent the most strenuous type of fault event given that the inductance offers little external damping with respect to the natural response of line connected machines [18].
The Converter Only Method

In contrast, the variable voltage source method of evaluating FRT capabilities consists of utilizing a high capacity power electronic converter in order to control the voltage at the point of common coupling with the device under test. Typically, this method is employed with a transformer connected to the power converter for voltage matching and isolation purposes. This is presently the case with respect to all multi-megawatt implementations and proposals of this technology [20], [21], [22]. It should be noted that, in this case, the voltage regulation is subject to the variable voltage source’s ability to compensate for the voltage drop across the impedance of the transformer and no direct zero impedance faults are possible.

Since the fault current associated with either synchronous or doubly fed induction generators can be upwards of six to eight times the rated current of the machine, the power converter must be capable of handling this short term overload. Additionally, due to the asymmetrical characteristics of the natural response of the fault current for these generators, the currents of individual semiconductor devices within the power converter are not evenly shared among the power electronic switching devices, greatly increasing the complexity of the power converter design. The common resultant of these design complexities is that these power converters tend to be unique designs – in many cases designed for a particular generator – that are specifically oriented towards only performing FRT evaluations.

The variable voltage source method does allow for a high degree of flexibility and controllability with respect to phase voltages, both during the fault event and during the subsequent recovery period. The main challenge associated with this method is that the point in which the fault is emulated is not at the point of common coupling with the device under test but, instead, at the terminals of the power electronic converter. Since this method has the impedance
of the voltage matching transformer, the control of the variable voltage source is required to simulate the fault impedance through the physical impedance of the transformer which is non-trivial if the fault impedance is small in magnitude and inductive in nature. Such would be the case with ZVRT testing. With respect to inductive fault impedances with high X/R ratios, the simulation of the fault impedance requires decoupling of AC and DC components in both the control system and the physical power converter to ensure proper damping effects of the natural response of the fault current. This can prove to be an impractically difficult problem to solve in a multi-megawatt power converter when coupled with the need for large overload capabilities and the relatively low bandwidth offered by low power electronic switching frequencies required for thermal management.

Additionally, because the point of creation of the fault event is at the terminals of the power electronic converter and not at the point of common coupling with the device under test, the impact of the transient voltage changes on the flux of the transformer must be taken into account, either by increasing the magnetic flux density capability of the transformer or by some method in which the flux within the transformer is managed. The first method of increasing the magnetic flux density capabilities of the transformer can prove to be a difficult engineering endeavor given the fact that the transformer design must balance the asymmetrical flux offset induced by the asymmetrical fault current of the device under test with the worst case excitation voltage changes required to simulate a fault at the terminals of the power electronic converter. Incorporating both of these challenges can result in a transform design that must be rated for 2 to 3 times the power of the system and can limit manufacturability due to this increased size and weight.
If the power electronic method of fault ride-through evaluations chooses to manage the excitation voltage transients such that the flux in the transformer is bounded, then the inherent trajectory and rate of change of such voltage transients is impacted. While management of the excitation voltage transients will meet the existing standards for fault ride-through evaluations, the inherent limitations imposed upon the voltage transitions will result in limiting the flux trapped within electrical machines that have line connected stators. The result of limiting the trapped flux is that the fault currents of the electrical machine will not fully exhibit the asymmetrical nature created by sharp voltage transitions.

The Hybrid Method

As demonstrated by the Venn diagram in Figure 2.5, the advantages of both of these technologies can be incorporated while minimizing their inherent limitations by merging both methods into a novel Hybrid Method for fault ride-through evaluations. The Hybrid Method, outlined in Figure 2.6, is achieved by coupling a variable voltage source to a reactive divider network with the goals of increasing the controllability of the reactive divider network while reducing short circuit duty required for implementation to a fraction of that of the two existing technologies described above. With respect to only the reactive divider network method, the impedance values of the series and shunt elements can be selected as a more reasonable value with respect to limiting the fault current from the variable voltage source. In addition, the series impedance can be compensated by the added control of the variable voltage source and subsequently, the short circuit duty required can be reduced. With respect to only the variable voltage source method, the short circuit duty is decreased because the shunt element of the
reactive divider network conducts a majority portion of the fault current in the system, noting that the corollary to a voltage divider circuit is a current division circuit.

While the Hybrid Method may appear as a straightforward marriage of two existing technologies, the underlying goal of reducing the short circuit duty required for implementation significantly changes the control problem with respect to maintaining the proper voltages prior to, during and after the fault event. Both the reactive divider network and the variable voltage source methods utilize shear power, in the form of short circuit duty, to overcome the fault characteristics of the device connected to the system, albeit in slightly different manners. The Hybrid Method of coupling a reactive divider network to a variable voltage source represents a departure from these existing brute-force methods and, through the implementation of novel control schemes, aims to simplify hardware design and scalability while maintaining the satisfactory degree of accuracy for FRT evaluations.
Because the fault is physically created with the reactive divider network at the point of common coupling with the device under test, a true zero fault impedance event is possible for ZVRT evaluations. If special care is taken in designing the reactive divider network, point-in-wave control and sharp voltage transitions are maintained and even enhanced from those found in typical reactive divider networks. Additionally, because the fault event is created at the point of common coupling and its electrical distance from the variable voltage source is determined by the series impedance, the excitation voltage of the transformer between the reactive divider network and the variable voltage source can be decoupled from the excitation voltage of the transformer of the device under test. Thus, the transformer of the device under test can be allowed to saturate while the transformer integral to the Hybrid Method can be kept from saturating. As demonstrated in [23], this issue of magnetic flux saturation during fault events is a contributing factor with regard to the evaluation of the device’s fault ride-through characteristics.

The research presented in this document will develop the basic physical system and vector control methods of the Hybrid Method in order to achieve the above objectives and provide a basis for future work with respect to the evaluation of multi-megawatt devices during fault events.
CHAPTER THREE
THE HYBRID METHOD: BASIS OF CONTROL

The single line diagram of the Hybrid Method physical system is shown in Figure 3.1 and contains the key elements of a variable voltage source, a voltage matching transformer, variable series impedance, series impedance bypass switches, variable shunt impedance and shunt impedance insertion switches. Figure 3.1 also illustrates the Point of Common Coupling (PCC) that is designated electrically as the point in the circuit in which the fault events are to be replicated.

The reactive divider network has been modified in two key ways with respect to circuits typically employed in the existing reactive divider network technologies. First, the variable series impedance includes a variable resistance in order to adjust the time constant of the series impedance. This serves the purpose of controlling the time constant associated with the attenuation of asymmetrical fault currents within the series impedance that are consistent with the natural response of inductive circuits to switching transients. The additional resistance results in minimal impact to the time constant associated with the parallel combination of the series and shunt impedances. The resistance also helps to ensure that the majority of the sub-harmonic content associated with the natural, asymmetrical fault characteristic response of the device under test is relegated to the shunt impedance.

The second modification involves the switches and switch types employed in the Hybrid Method as presented here. A series bypass switch is actively utilized in the Hybrid Method for the purposes of increasing the controllably and functionality of the circuit. The switch types have been modified from mechanically operated, medium voltage circuit breakers used in existing implementations of the reactive divider network to power electronic, thyristor based AC
switches. The purpose for utilizing thyristor based switches is that thyristors have a natural commutation to the off state near a zero crossing of the current. Further, thyristors can be turned on with much better accuracy than mechanical switches. This improved switching time allows for better performance with respect to the point-in-wave that the switch is closed, which is critical for fault evaluations in general and in inductive circuits that employ zero current switching.

![Diagram of Hybrid Method physical system](image)

**Figure 3.1:** The figure depicts the single line diagram of the Hybrid Method physical system. The key elements of the circuit are a variable voltage source, a voltage matching transformer, variable series impedances, series impedance bypass switches, variable shunt impedances and shunt impedance insertion switches.

In the Hybrid Method, the series and shunt impedances are discretely variable based upon the per-unit voltage and power of the system. The series and shunt inductances are such that they are adjustable in increments of 5% of the base impedance, where the base impedance is designated by the rated power and voltage of the variable voltage source. The total summation of the series and shunt inductances can be up to 125% of the base impedance for increased flexibility. Air-core inductors will mitigate residual flux and saturation issues. The series
resistance is also discretely variable with a total resistance such that the time constant of the total resistance with an inductive impedance of 100% of the base impedance is equal to one fundamental cycle of the highest nominal system frequency. The highest nominal frequency is assumed to be 60 Hz and the resistor is selected to be discretely variable with respect to one fifth of the total resistance. The practical implementation of the discretely variable impedances will be discussed later in this chapter.

Neglecting the resistive component, such discretely variable inductances allow for over 300 possible combinations of series and shunt inductances, yielding a high degree of flexibility in selection of impedances for fault ride-through evaluations. Physical constraints and construction practices may dictate slight deviations from these values and it can be shown that these deviations are of little consequence with respect to the performance as long as the parameters can be identified.

Important factors with respect to the implementation of the Hybrid Method are the characteristics of the variable voltage source and those of the voltage matching transformer. The variable voltage source and the transformer must both be capable of producing and transmitting zero sequence voltage. This implies that the variable voltage source, which is inherently a power electronic converter, cannot be a standard three wire power converter topology, and the most suitable topology for the variable voltage source would be a series connected H-bridge power converter [24], [25], [26], [27]. Additionally, the voltage matching transformer must have physical design characteristics that support zero sequence flux within the core structure. Such transformer characteristics can be achieved by using a three phase, 5-limb, core or shell type, or by using three single phase transformers [28], [29], [30].
Additionally, the variable voltage source must have continuous overvoltage capabilities in order to support the controllability of the Hybrid Method when large series impedances are coupled with high device fault duties. The overvoltage capabilities are to be utilized in compensating for the voltage drop across the series impedance and allow for the capability to create voltage recovery overshoot scenarios typical of some types of fault events [11]. Subsequently, the transformer must also be capable of handling these continuous overvoltage events with minimal magnetic saturation. If the variable voltage source is a multi-level series connected H-bridge (SCHB) power converter topology, the harmonic content of the converter is greatly reduced and the implementation of a vector control system based upon the fundamental frequency is more realizable because the control system need not fight its own harmonic content.

Figure 3.2 demonstrates the operation cycle of the Hybrid Method for creating a fault at the point of common coupling (PCC). Initially the reactive divider network is bypassed by the series bypass switch and the PCC is tightly coupled to the variable voltage source through the low impedance of the transformer. Then at Step 1, the series bypass switch is opened in order to insert the series impedance into the circuit and the variable voltage source will then be loosely coupled to the PCC, requiring compensation of the voltage drop across the series impedance by the variable voltage source in order to regulate the voltage at the PCC. To initialize the fault, the shunt fault switch is closed in Step 2, inserting the shunt impedance into the circuit. Then the operation continues in reverse order by opening the shunt fault switch to remove the shunt impedance from the circuit in Step 3, clearing the fault. Finally, in Step 4 the series impedance is again bypassed by closing the series bypass switch, which returns the system to normal unfaulted operation where the PCC is tightly controlled by the variable voltage source.
Figure 3.2: This figure demonstrates the operation cycle of the Hybrid Method. The operation cycle is as follows: starting at the left with the series impedance bypassed, to the bottom with the series impedance inserted, to the right with the shunt impedance inserted, to the top with the shunt impedance removed, and back to the left with the series impedance bypassed.

It is important to note that the fault impedance is only inserted into the circuit when the series impedance is already in the circuit as this will greatly reduce the complexity of the control required. It is evident from Figure 3.2 that the system has three distinct states and that operation requires cycling through them in the manner shown. The implementation of the vector control algorithm will utilize this operation cycle.
This section will focus on the single phase system of equations as they relate to the physical model of the Hybrid Method. Fundamentally, the actual system is a three phase system and will result in cross coupling between phases for specific fault types. However, the single phase equivalent circuit is suitable to demonstrate the characteristics of the Hybrid Method that are advantageous with respect to the design goal of limiting the required fault duty of the variable voltage source.

Figure 3.3 demonstrates the single phase representation of the Hybrid Method as well as the Thevenin equivalent circuit that will be used for analysis and development of the control strategy. With reference to the equivalent circuit in Figure 3.3, allowing the transformer winding resistance to be represented by $R_X$ and the leakage inductance to be represented by $L_X$, the linear, time varying system of equations can be developed for the single phase equivalent circuit.

![Diagram](image)

Figure 3.3: (a) A single phase representation of the complete circuit including the switching devices. (b) A single phase Thevenin equivalent circuit with time varying elements that represent the time varying nature imposed by the switch states.
Starting with the single phase representation, the equations for the output voltage at the point of common coupling given the specific switch states corresponding to the operation of the Hybrid Method are given by equation 3.1 when the series bypass switch is closed and by equation 3.2 when the series bypass switch is opened to insert the series impedance. By letting the output current be expressed as in equation 3.3, the output voltage at the point of common coupling when the shunt fault switch is closed is given by equation 3.4.

\[
V_o(s) = V_s(s) + (R_X + sL_X)I_o(s) \quad 3.1
\]

\[
V_o(s) = V_s(s) + (R_S + R_X + s(L_S + L_X))I_o(s) \quad 3.2
\]

\[
I_o(s) = I_s(s) + I_F(s) \quad 3.3
\]

\[
V_o(s) = \left(\frac{sL_F}{R_S + R_X + s(L_S + L_X + L_F)}\right)V_S(s) + \left(\frac{sL_F(R_S + R_X + s(L_S + L_X))}{R_S + R_X + s(L_S + L_X + L_F)}\right)I_o(s) \quad 3.4
\]

Equation 3.4 demonstrates the classic voltage divider circuit given the source voltage and the equivalent Thevenin impedance with respect to the output current. Recognizing the corollary between a traditional voltage divider circuit and the subsequent current division, it is clear that the Thevenin impedance plays an important role with respect to the short circuit duty seen by the variable voltage source. Combining the three system equations (3.1, 3.2, and 3.4) into one complete system equation with respect to the physical system is given by equation 3.5, where \(M(s, t)\) is given by equation 3.6 and \(N(s, t)\) is given by equation 3.7.

\[
V_o(s) = M(s, t)V_S(s) + N(s, t)I_o(s) \quad 3.5
\]

\[
M(s, t) = \begin{cases} 
1, & S_F \text{ open} \\
\frac{sL_F}{R_S + R_X + s(L_S + L_X + L_F)}, & S_F \text{ closed}
\end{cases} \quad 3.6
\]
In these equations, \( M(s, t) \) represents the time varying nature of the Thevenin voltage with respect to the state of the shunt fault switch and \( N(s, t) \) represents the time varying nature of the Thevenin impedance with respect to the states of both the series bypass switch and the shunt fault switch. From the basic Thevenin equivalent circuit, it is clear that \( M(s, t) \) represents the open circuit voltage division of the system, while \( N(s, t) \) corresponds directly to the closed circuit voltage drop across the Thevenin impedance. It is important to remember the operation cycle of the Hybrid Method presented earlier in this chapter because the above equations assume that the series bypass switch is always open when the shunt fault switch is enabled. This time varying Thevenin equivalent system will be further elaborated on later in this chapter to incorporate the three phase nature of the system and serves as the basis of design with respect to developing control strategies and objectives in the next section.

**Development of the Control Strategy**

This section will utilize the system equations of the Hybrid Method developed in the previous section to derive the control objectives and strategy. The primary control objective of the Hybrid Method for performing fault evaluations is regulation of the voltage at the point of common coupling prior to, during and after the fault. This section will develop the understanding of how the independent system and control variables and the dependent control variables contribute to the operation and performance of the Hybrid Method. The ultimate
control of the Hybrid Method will result in complete phase independence in both the physical system and the control system, allowing for more flexibility with unsymmetrical fault scenarios.

The independent system variables are the series and shunt impedances, the independent control variables are the phase reference voltages and the dependent control variables are the phase voltages generated by the variable voltage source. This section will introduce the concept of a vector control strategy by constraining the equations governing the basis of the control to the fundamental frequency, allowing for the physical system equations and control equations to be simplified to complex vectors instead of time domain transfer functions.

Because the purpose for developing the Hybrid Method is to limit the short circuit duty required by the variable voltage source, the current injected by the device under evaluation at the point of common coupling will play a significant role in voltage regulation at the point of common coupling. This is especially true given the fault characteristics of the electrical machine types presented earlier, where instantaneous peak currents can be over six times the nominal machine current with rapid exponential decay during the fault event. Further complicating the regulation problem is the asymmetrical nature of the fault currents as they pass through the frequency dependent impedances of the reactive divider network.

Building upon the time varying Thevenin equivalent circuit in the previous section, the basis of control can be implemented according the Internal Model Principle. Naturally, the Internal Model Principle suffers from parametric uncertainty between the physical system and the internal model utilized for control. With respect to implementation of the Hybrid Method, the physical system is composed of measureable quantities that, when constrained to a single frequency of a vector control application such as the one presented here, tend to be well behaved. Nevertheless, prior to any physical implementation, the uncertainty of the measured values of the
impedances must be taken into account when evaluating the overall system accuracy but with respect to the stability and controllability of the Hybrid Method, the uncertainty has a negligible effect.

As outlined in the previous section, the time varying nature of the physical system caused by the switch states can be handled as well defined disturbances that are known a priori with respect to manipulation of the control variable. In this system, the control variable is the output voltage of the variable voltage source, represented in the following equations by $V_{Sc}(s)$. Adhering to the Internal Model Principle, the system equation developed in the previous section can be solved for the control variable, resulting in equation 3.8, where $K(s,t)$ and $G(s,t)$ are defined for each switch state in equations 3.9 and 3.10, respectively.

$$V_{Sc}(s) = K(s,t) V_{Or}(s) - G(s,t) I_{om}(s) \tag{3.8}$$

$$K(s,t) = M^{-1}(s,t) = \begin{cases} R_s + R_X + s(L_s + L_X + L_F) \over sL_F & S_F \text{open} \\ \frac{1}{S_F \text{closed and } S_B \text{closed}} & \end{cases} \tag{3.9}$$

$$G(s,t) = M^{-1}(s,t) N(s,t) = \begin{cases} \frac{R_X + sL_X}{R_X + R_S + s(L_X + L_S)} & S_B \text{open} \\ \frac{1}{S_B \text{closed}} & \end{cases} \tag{3.10}$$

Equation 3.8 demonstrates the summation of the two distinct control variables that contribute to the primary control variable. The open circuit, open loop response of the system is set by the reference output voltage, $V_{Or}(s)$, multiplied by the inverse of the voltage divider function, $K(s,t)$. The closed circuit response of the control variable is equal to the feedback of the measured output current $I_{om}(s)$ multiplied by the Thevenin impedance, $G(s,t)$, and serves as an indirect measure of the voltage drop in the Thevenin equivalent circuit. From equation 3.9, $K(s,t)$ is dependent only upon the state of the shunt fault switch and, from equation 3.10, $G(s,t)$ is only dependent upon the state of the series bypass switch.
The separation of the control variable into a feed-forward output voltage reference, 
\( K(s, t) V_{OR}(s) \), and a feedback voltage compensation term, \( G(s, t) I_{OM}(s) \), is very beneficial
with respect to transitions of the switch states, development of control strategies for the hybrid
system, and implementation of a vector control method. It should be noted that only the output
current of the device under test is measured in this implementation and thus the amount of
sensing required of the control system is limited. Inherently, some of the challenges of this
implementation of the Hybrid Method could warrant more than one measurement point in order
to increase the overall system performance and accuracy but it is not required for stability and
controllability.

For implementation of a vector control strategy, the system needs to be constrained to the
fundamental frequency such that the continuous time functions of \( K(s, t) \) and \( G(s, t) \) can be
represented as the complex vectors \( K(j\omega, t) \) and \( G(j\omega, t) \) that are time variant in magnitude and
phase upon only the switch states. In order to constrain the control variables to the fundamental
frequency, the control system must contain a method of band-pass filtering the control variable.
This will be expanded upon in the Chapter Five where methods of band-pass filtering will be
explored with respect to passively managing the flux of the transformer between the variable
voltage source and the reactive divider network.

Recognizing that the control variable can be constrained to the fundamental frequency for
vector control, it is helpful to review an example fault scenario to look into the various aspects of
the control strategy with respect to the independent and dependent variables. Figure 3.4
demonstrates an example symmetrical fault scenario and outlines the operation cycle of the
Hybrid Method with respect to the control variable (the output voltage of the variable voltage
source) and the reference voltage (the voltage at the point of common coupling). Figure 3.4
depicts the voltage compensation of the control variable in order to counteract the voltage drop across the series impedances and force the output voltage near to the reference voltage for the given output current. The output current of the device is assumed and is not shown in the figure for clarity.

At time zero in Figure 3.4, the shunt fault switch is closed in order to initiate the fault event. During the fault, the control variable is calculated as the summation of both the feed-forward voltage reference, which can deviate from the nominal voltage reference, and the feedback voltage compensation of the equivalent Thevenin impedance. The main purpose of manipulating the feed-forward voltage reference during the fault is to limit the open circuit fault current characteristic based upon the series and shunt impedances utilized in the specific fault scenario.
The fast output voltage transitions required of the variable voltage source is a particularly important issue as demonstrated in the locus in the bottom right of Figure 3.4. When a voltage matching transformer is utilized, the flux within the core of this transformer must be managed and bounded in order to limit the possibility of magnetic saturation within the transformer. Chapter Five will discuss this issue in more detail. Because the point of the fault being created is at the point of common coupling and is electrically distant from the transformer connected to the variable voltage source by the series impedance, the mutual excitation with the transformer of the device under test is minimized. The transformer connected to the variable voltage source will see the fault event more as a simple load step change but the transformer of the device under test will see dramatic changes in the excitation voltage that can result in magnetic saturation.

The main challenge associated with the control equations developed in this section is enforcing the practical limitations, rated voltage and current, of the physical variable voltage source with the fault characteristics of unknown machine types. From equation 3.8, one can easily envision, given a fault scenario with an induction machine, that the collapse of the machine excitation during the fault will result in a large reactive power draw once the voltage attempts to recover after the fault. Using even moderate series impedance, the reactive power drawn by the recovering induction machine will promote voltage collapse at the point of common coupling. In order to counteract this voltage collapse, the variable voltage source should be capable of dynamically producing continuous terminal voltages greater than the rated voltage at the point of common coupling such that the voltage at the point of common coupling can be supported while the field is re-established on the induction machine. In practice, this will result in over-sizing of the variable voltage source such that it is capable of 130% to 145%
continuous rated overvoltage such that the appropriate dynamic range is available for voltage regulation both during and after the fault event.

The other issue is associated with the current seen by the variable voltage source and how to constrain equation 3.8 such that a current limit is imposed upon the variable voltage source. Given that the current seen by the variable voltage source can be computed from a node voltage equation using the variable voltage source output voltage and the voltage at the point of common coupling, application of saturation to the feedback voltage compensation term, \( G(s, t) I_{OM}(s) \), can effectively act to limit the current seen by the amplifier. One clear example of why this saturation is required is during a zero voltage fault scenario at the point of common coupling where the shunt impedance is negligible and an appreciable amount of fault current being delivered by the device under test. By equation 3.10, the feedback voltage compensation would be calculated based upon the series impedance and could be appreciable given even small amounts of series impedance. However, given the lack of leverage of the variable voltage source on the voltage at the point of common coupling calculated by equation 3.4, the commanded voltage from the variable voltage source could act to send the variable voltage source into overcurrent as it attempts to regulate a very small voltage. This scenario represents a more obvious limitation that is corrected by constraining the feedback voltage compensation.
Three Phase System of Equations

Up to this point, the focus has been on the basic demonstration of the Hybrid Method through single line diagrams, the operation cycle, and specific system characteristics. While these equations may be sufficient for symmetrical three-phase faults, they do not properly capture the behavior of the system for all types of unsymmetrical faults. In order to derive the system equations and investigate the Hybrid Method’s capability of unsymmetrical fault evaluations, a three-phase diagram of the physical system is shown in Figure 3.5.

From Figure 3.5, it is evident that the Hybrid Method is capable of unsymmetrical faults, including: single line-to-ground faults (SLGF), double line-to-ground faults (DLGF), and line-to-line faults (LLF). These unsymmetrical fault cases are made possible by the fact that the shunt fault switches can be operated on an individual phase basis and that a neutral switch is employed to connect the common point of the shunt impedances to the neutral for SLGF and DLGF or the neutral switch is opened to allow for a LLF with a floating center point.
Figure 3.5: The three phase circuit schematic of the Hybrid Method for fault evaluations.

Equation 3.11 represents the three-phase, Thevenin equivalent circuit of the system, where \( M(s,t) \) and \( N(s,t) \) can be derived based upon the unsymmetrical nature of the fault characteristic. To be mathematically correct, the matrices are written as linear time varying functions since the physical system cannot be constrained to only the fundamental frequency. While these matrices are diagonal for symmetrical and ground faults, a line to line fault will result in off-diagonal terms indicating the cross coupling between phases that are to be expected. However, if the physical and control systems are phase independent, then the introduction of the cross coupling terms are of little consequence with respect to offering voltage regulation at the point of common coupling because the cross coupling terms cancel out in the resulting equations.

\[
\begin{bmatrix}
V_{OA} \\
V_{OB} \\
V_{OC}
\end{bmatrix} = M(s,t) \begin{bmatrix} V_S \end{bmatrix} + N(s,t) \begin{bmatrix} I_O \end{bmatrix}
\]

Similiar to the single phase derivation of the control variable, equation 3.12 represents the three phase control variables with respect to the matrices \( K(j\omega, t) \) and \( G(j\omega, t) \). Again, these
matrices are diagonal for symmetrical and ground faults, and \( K(j\omega, t) \) contains off diagonal terms for line to line faults. However, \( K(j\omega, t) \) and \( G(j\omega, t) \) can be constrained to the fundamental frequency components by the band-pass nature of the vector controller and can be represented by time varying complex vectors.

\[
\begin{bmatrix}
V_{SCA} \\
V_{SCE} \\
V_{SCC}
\end{bmatrix} = K(j\omega, t) \begin{bmatrix}
V_{OBA} \\
V_{OBB} \\
V_{OBC}
\end{bmatrix} - G(j\omega, t) \begin{bmatrix}
I_{OMA} \\
I_{OMB} \\
I_{OMC}
\end{bmatrix}
\]

Exactly like the single phase system, the time varying nature of \( K(j\omega, t) \) corresponds to the state of the shunt fault switches on a per phase basis and the time varying nature of \( G(j\omega, t) \) corresponds to the state of the series bypass switches on a per phase basis.

Since the Hybrid Method must operate under severe voltage and current imbalance, the control strategy is unable to further constrain the system to specific vector spaces based upon limiting the degrees of freedom of the physical system. More specifically, for the Hybrid Method to create unsymmetrical faults, the control system must properly account for zero sequence voltages and currents. Therein, the common practice in power converter control of eliminating the zero sequence current by restricting the physical system to only three wires is unacceptable for the Hybrid Method. Additionally, the transformer coupling the variable voltage source to the reactive divider network should also be capable of passing a zero sequence voltage of at least one third of the rated positive sequence voltage. This level of zero sequence voltage would be equivalent to a sustained SLGF in which the voltage in a single phase is zero.

With this, the only differences in regards to specific vector spaces for the analysis of the system and the implementation of the control strategy would come from using a vector space that transforms the system into an orthogonal base. Such vector spaces would include the symmetrical component phasor vector space common for fault analysis, and the stationary or
rotating vector spaces (Clarke and Park transformations respectively) common to motor drive applications and electrical machine control. Since the system being described is relatively small, transforming the system to symmetrical components is of little value, especially given the fact that symmetrical component analysis is typically done in the phasor domain with constant impedances. This assumption is very different than the exponentially decaying, asymmetrical fault currents one can expect from some machine types (e.g., synchronous or doubly-fed) with the Hybrid Method. Also, because symmetrical fault analysis requires phasor form of the signals, there is both added control burden and time delay associated with the conversion to a complex phasor.

While the utilization of stationary and rotating reference frames tends to simplify the model and control of electrical machines by eliminating the time varying inductances, they will work only to obfuscate the equations relating to the Hybrid Method. This is especially true given the fact that the Hybrid Method will require zero sequence voltage and current control which is almost universally neglected in vector control applications since the systems are normally three-wire systems. Additionally, the control applications with stationary or rotating reference frames are uniquely sensitive to harmonic components as different harmonic frequencies and components tend to gravitate towards different vectors in the transformation. Nevertheless, it is possible that a controller could be developed upon any of these vector spaces that would allow for all of the capabilities required, but it is not warranted given the ease of implementation of the derived three-phase systems of equations.

Knowing the general format for the three-phase systems of equations for representing and controlling the Hybrid Method (Equations 3.11 and 3.12) the matrices for the three phase implementation for symmetrical and unsymmetrical fault scenarios can be derived. In the
following matrices, the simplification of allowing the series impedance to be equal to Z\textsubscript{S} and the shunt impedance to be equal to Z\textsubscript{F} has been made. The series and shunt impedances are also presumed to be equal on all phases. These matrices assume that the shunt impedance is in the circuit, implying that the series bypass switches are open and the shunt fault switches indicated by the faulted phases are closed.

Figure 3.6 demonstrates the simplified schematic of a symmetrical three-phase fault and equations 3.13 and 3.14 represent the physical system and controller matrices for this fault, respectively.

![Figure 3.6: The circuit schematic of a three phase fault that is grounded at the neutral point of the shunt impedance.](image)

\[
M = \begin{bmatrix}
\frac{Z_F}{Z_F + Z_S} & 0 & 0 \\
0 & \frac{Z_F}{Z_F + Z_S} & 0 \\
0 & 0 & \frac{Z_F}{Z_F + Z_S}
\end{bmatrix}
\]

\[
N = \begin{bmatrix}
\frac{Z_S Z_F}{Z_F + Z_S} & 0 & 0 \\
0 & \frac{Z_S Z_F}{Z_F + Z_S} & 0 \\
0 & 0 & \frac{Z_S Z_F}{Z_F + Z_S}
\end{bmatrix}
\]

\[
K = \begin{bmatrix}
\frac{Z_S + Z_F}{Z_F} & 0 & 0 \\
0 & \frac{Z_S + Z_F}{Z_F} & 0 \\
0 & 0 & \frac{Z_S + Z_F}{Z_F}
\end{bmatrix}
\]

\[
G = \begin{bmatrix}
Z_S & 0 & 0 \\
0 & Z_S & 0 \\
0 & 0 & Z_S
\end{bmatrix}
\]
Figure 3.7 demonstrates the simplified schematic of a double line to ground fault (DLGF) and equations 3.15 and 3.16 represent the physical system and controller matrices for this fault, respectively.

![Double Line to Ground Fault Schematic]

Figure 3.7: The circuit schematic of a double line to ground fault on phases A and B.

\[
M = \begin{bmatrix}
\frac{Z_F}{Z_F + Z_S} & 0 & 0 \\
0 & \frac{Z_F}{Z_F + Z_S} & 0 \\
0 & 0 & 1
\end{bmatrix}
\]

\[
N = \begin{bmatrix}
\frac{Z_S Z_F}{Z_F + Z_S} & 0 & 0 \\
0 & \frac{Z_S Z_F}{Z_F + Z_S} & 0 \\
0 & 0 & Z_S
\end{bmatrix}
\]

\[
K = \begin{bmatrix}
\frac{Z_S + Z_F}{Z_F} & 0 & 0 \\
0 & \frac{Z_S + Z_F}{Z_F} & 0 \\
0 & 0 & 1
\end{bmatrix}
\]

\[
G = \begin{bmatrix}
Z_S & 0 & 0 \\
0 & Z_S & 0 \\
0 & 0 & Z_S
\end{bmatrix}
\]

Figure 3.8 demonstrates the simplified schematic of a single line to ground fault (SLGF) and equations 3.17 and 3.18 represent the physical system and controller matrices for this fault, respectively.
Figure 3.8: The circuit schematic of a single line to ground fault on phase A.

\[
M = \begin{bmatrix}
Z_F & 0 & 0 \\
Z_F + Z_S & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1 \\
\end{bmatrix} \quad \quad N = \begin{bmatrix}
Z_S Z_F & 0 & 0 \\
\frac{Z_S Z_F}{Z_F + Z_S} & 0 & 0 \\
0 & Z_S & 0 \\
0 & 0 & Z_S \\
\end{bmatrix}
\]

3.17

\[
K = \begin{bmatrix}
\frac{Z_S + Z_F}{Z_F} & 0 & 0 \\
0 & 1 & 0 \\
0 & 0 & 1 \\
\end{bmatrix} \quad \quad G = \begin{bmatrix}
Z_S & 0 & 0 \\
0 & Z_S & 0 \\
0 & 0 & Z_S \\
\end{bmatrix}
\]

3.18

Figure 3.9 demonstrates the simplified schematic of a line to line fault (LLF) and equations 3.19 and 3.20 represent the physical system and controller matrices for this fault, respectively.

Figure 3.9: The circuit schematic for a line to line fault between phases A and B.
The one theme common to all of the fault types presented above is that the feedback compensation impedance matrix is consistent between them, regardless of the fault type being created. This implies that the complex saturation of the feedback compensation voltage does not necessarily need to be adjusted for each fault type. This also infers that adjustments can be made to the feed-forward voltage reference during the fault in order to promote lower open circuit fault currents for even the off-diagonal terms of the line to line fault.

\[
M = \begin{bmatrix}
\frac{Z_S + Z_F}{Z_F + 2Z_S} & \frac{Z_S}{Z_F + 2Z_S} & 0 \\
\frac{Z_S}{Z_F + 2Z_S} & \frac{Z_S + Z_F}{Z_F + 2Z_S} & 0 \\
0 & 0 & 1
\end{bmatrix} \quad N = \begin{bmatrix}
\frac{Z_S(Z_S + Z_F)}{Z_F + 2Z_S} & \frac{Z_S^2}{Z_S(Z_S + Z_F)} & 0 \\
\frac{Z_S^2}{Z_S(Z_S + Z_F)} & \frac{Z_S(Z_S + Z_F)}{Z_F + 2Z_S} & 0 \\
0 & 0 & \frac{Z_S}{Z_S}
\end{bmatrix} \quad 3.19
\]

\[
K = \begin{bmatrix}
\frac{Z_S + Z_F}{Z_F} & -\frac{Z_S}{Z_F} & 0 \\
-\frac{Z_S}{Z_S + Z_F} & \frac{Z_S + Z_F}{Z_F} & 0 \\
0 & 0 & 1
\end{bmatrix} \quad G = \begin{bmatrix}
Z_S & 0 & 0 \\
0 & Z_S & 0 \\
0 & 0 & Z_S
\end{bmatrix} \quad 3.20
\]
CHAPTER FOUR
THE HYBRID METHOD: PHYSICAL SYSTEM

This chapter will focus on the practical implementation of the physical system with respect to the Hardware-In-the-Loop Grid Simulator project [31] to be co-located with the Wind Turbine Drivetrain Testing Facility (WT-DTF) at the Clemson University Energy Systems Testing Facility in North Charleston, SC [32]. The detailed implementation and specifications of the individual components, including: the variable voltage source, the voltage matching transformer, the reactive divider network and the medium voltage, solid-state AC switches, will be discussed with regard to the design of the Hybrid Method.

Ultimately, the information presented in this chapter will be utilized to implement the physical system model and vector control algorithm that will both be executed on separate pieces of hardware in real-time against simulated devices in order to validate the fault ride-through evaluation capabilities of the system. This chapter is presented such that the complete physical system can be realized in order to better understand the limitations of the individual components involved and to justify some of the modeling concessions that must be made when simulating the physical system on a Real Time Digital Simulator (RTDS).

The continuous power rating of the complete physical implementation of the Hybrid Method is 15 MVA at 23.8 kV. However, this does not indicate the transient fault duty capabilities of the complete Hybrid Method physical system. Figure 4.1 demonstrates the thermal and voltage isolation boundaries of the reactive divider network with respect to the fault capabilities of the Hybrid Method physical system. The voltage isolation is set as 100 MVA with respect to the voltage at the point of common coupling, 23.9 kV and the thermal boundary is limited by the air core reactors that make up reactance in the reactive divider network.
Figure 4.1: The thermal and voltage isolation boundaries of the Hybrid Method Reactive Divider Network overlaid on the most restrictive LVRT and HVRT boundaries.

With respect to the components for the implementation of the Hybrid Method, it must be noted that several of the limitations are imposed because the complete system is being designed to handle a multitude of grid integration evaluations. These evaluations are outlined in Table 4.1. Several of these grid integration evaluations require more sophisticated equipment, especially with respect to the variable voltage source. These more sophisticated requirements have been driving factors in the development of the Hybrid Method because the oversized power electronic converters utilized in converter only methods of fault ride-through evaluations do not have the bandwidth or harmonic characteristics required for proper harmonic evaluations nor for detailed transient hardware-in-the-loop studies.
The following sections will discuss the theory behind the specifications of the physical equipment utilized to implement the Hybrid Method. The specifications, functionality, and underlying design assumptions made in this chapter are a combined effort between the author, the Clemson University Hardware-In-the-Loop Grid Simulator team, and the respective suppliers of each piece of equipment. However, the application of these devices to a functional and controllable Hybrid Method of performing fault ride-through analysis is the sole work of the author.

**Medium Voltage, Multi-Level Power Amplifier**

This section will discuss the physical implementation of the variable voltage source which is a key element in the success of the Hybrid Method. Up to this point, the variable voltage source has been assumed to be linear but, in fact, this variable voltage source will be a medium voltage, multilevel power electronic converter based upon a Series Connected H-Bridge (SCHB) topology, alternatively referred to in this work as a power amplifier. The rated power of the SCHB power electronic converter to be utilized as the variable voltage source is 15 MVA at

<table>
<thead>
<tr>
<th>Table 4.1: Possible Grid Integration Evaluations to be Implemented with the Same Physical System as the Hybrid Method.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Steady State</strong></td>
</tr>
<tr>
<td>• Power Set Points</td>
</tr>
<tr>
<td>• Voltage Variations</td>
</tr>
<tr>
<td>• Frequency Variations</td>
</tr>
<tr>
<td>• Controls Evaluation</td>
</tr>
</tbody>
</table>

45
4.16 kV. Many of the fundamental specifications and operation details presented here can also be found in [33].

For any power electronic converter, the converter is separated into three fundamental components, the input converter that converts AC to DC, the DC bus, and the output converter that converts the DC back into variable frequency, variable voltage AC. Since the power electronic converter to be utilized as the variable voltage source must inherently be four-quadrant capable, the input converter is an active front end that can absorb and deliver real and reactive power from the interconnection with the utility source. However, to better understand the characteristics and design of the SCHB topology, it is easier to start with the output converter(s) and work backwards to the interconnection with the utility source.

At the most fundamental level, the series connected H-bridge topology consists of series connected single-phase voltage sources if it is assumed that each individual pulse width modulation (PWM) controlled H-bridge is an independent, linear source. Figure 4.2 demonstrates the concept of four independent linear sources stacked in series per phase, with the phases connected in a wye configuration. The wye configuration is extremely important because it allows for four wire operation, meaning that the SCHB topology is naturally able to source zero sequence voltage as long as the phase voltages can be varied independently. Likewise, the SCHB topology could utilize a delta configuration but this is more commonly encountered in modular multilevel converter (MMC) technologies for HVDC applications where there is no bulk DC bus capacitance.
Figure 4.2: An approximate equivalent circuit model of a three phase Wye, series connected H-bridge (SCHB) power converter consisting of four series connected voltage sources per phase.

Removing the assumption that the individual power electronic sources are linear, Figure 4.3 demonstrates the SCHB topology comprised of individual H-bridge PWM converters. Each individual H-bridge PWM converter has its own isolated DC supply such that they can be stacked in series or connected in parallel. The H-bridge PWM converters are grouped by output phase sets of three into slices for active front end diversification, modularity, and isolation purposes.

Figure 4.4 demonstrates the active front end connections at the slice level, where the three active front ends consist of three phase PWM converters connected to three isolated low voltage windings of a four winding transformer. The transformer provides the isolation between all three phases of the output H-bridge PWM converters. Slice to slice isolation is also provided by the transformer, thus slices can be connected with series output H-bridge PWM converters and parallel input PWM converters. Ultimately, the maximum number of series output H-bridge PWM converters that can be connected in series is a function of the isolation voltage between transformer secondary windings and the slice to slice isolation. For this specific purpose, the rated voltage isolation is such that up to 12 H-bridge PWM converters can be connected in series.
The electrical characteristics of each SCHB power electronic converter cabinet to be utilized as the variable voltage source can be found in Table 4.2, where the cabinet consists of two, four slice SCHB converters that have their outputs connected in parallel. For the rated output voltage at rated power, only three H-bridge PWM converters are needed to be connected in series per phase and the fourth H-bridge is utilized to achieve a 130% continuous overvoltage capability of the SCHB power electronic converter.
Table 4.2: The Electrical Characteristics of the Individual Series Connected H-Bridge Power Electronic Converters

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power</td>
<td>3.75 MVA</td>
</tr>
<tr>
<td>Input Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Primary Input Voltage</td>
<td>4.16 kV</td>
</tr>
<tr>
<td>Secondary Voltage</td>
<td>620 V</td>
</tr>
<tr>
<td>Rated H-Bridge Output Voltage</td>
<td>740 V</td>
</tr>
<tr>
<td>Rated Output Voltage</td>
<td>4.16 kV</td>
</tr>
<tr>
<td>Maximum Output Voltage</td>
<td>5.125 kV</td>
</tr>
<tr>
<td>DC Bus Voltage</td>
<td>1100 V</td>
</tr>
<tr>
<td>AFE Switching Frequency</td>
<td>2 kHz</td>
</tr>
<tr>
<td>Output Switching Frequency</td>
<td>0.6 - 2 kHz</td>
</tr>
<tr>
<td>Rated Output Current</td>
<td>300 A</td>
</tr>
<tr>
<td>Momentary Overload</td>
<td>200%</td>
</tr>
<tr>
<td>Sustained Overload (1 min)</td>
<td>110%</td>
</tr>
</tbody>
</table>

Figure 4.4: A schematic of the three active front ends connected to a three-phase, 4 winding transformer.
In order to scale the 3.75 MVA sections of the base SCHB power electronic converter into 15 MVA, four of the cabinets are connected in parallel as demonstrated in Figure 4.5. The four cabinets are grouped by pairs onto two separate 7.5 MVA transformers. This is included in order to allow the system to circulate power within itself and to be segmented into smaller subsystems. Including the fact that each individual section has a fourth H-bridge utilized for overvoltage capabilities, the true rating of each cabinet is actually 5 MVA and the overall power amplifier is technically rated for 20 MVA that is nominally run near 75% of its rated capacity for the nominal steady-state “nameplate” rating.

![Diagram of power amplifier layout](image)

Figure 4.5: A single line diagram of a 20 MVA SCHB power amplifier that consists of two independent parallel power splits with their own respective input and output transformers. Within each of the two power splits, there are four parallel SCHB power amplifiers split between two cabinets, making for a total of eight parallel SCHB power amplifiers. Each of the eight parallel SCHB power amplifiers is rated for a 4160V input and a 5400 V output at 2.5 MVA.
One of the main advantages to utilizing multilevel power converter topologies is the voltage stepped waveforms that can be achieved with these topologies, resulting in a better resolved sinusoidal output voltage. With respect to the multilevel aspects of the series connected H-bridge converter, the number of phase voltage levels is given by equation 4.1 and the number of phase to phase voltage levels is given by equation 4.2. Thus, for the given application with four H-bridges connected in series, the number of phase voltage levels is 9 and the number of phase to phase voltage levels is 17 and, at nominal voltage, the number of levels are 7 and 13, respectively.

\[ L_\varphi = K + 1 : K = \text{Number of Series Connected Bridges} \]  
\[ L_{ll} = L_\varphi(2N - 1) \]

In addition, the lower order harmonic content of multilevel topologies can be pushed much farther out into the harmonic spectrum with advanced PWM techniques. This is especially true with a series connected H-bridge converter where phase shifted carrier pulse width modulation (PSCPWM) can be used [34]. As the name implies, the PSCPWM technique relies on phase shifting the triangle wave carriers between the individual H-bridges connected in series. The fundamental equation for the phase angle that the carriers should be shifted by is given in equation 4.3 [35]. Figure 4.6 demonstrates these phase shifted carrier waveforms for the four series connected H-bridges used in this application. As with typical carrier based PWM applications, the frequency of the triangle wave determines the switching frequency of the individual power electronic switching devices.

\[ \theta_{\text{carrier}} = \frac{180^\circ}{K} : K = \text{Number of Series Connected Bridges} \]
Figure 4.6: The triangle carrier waves required for Phase Shifted Carrier PWM (PSCPWM) with four independent H-bridge converters per phase.

Given that one of the benefits associated with the SCHB topology is that low voltage power electronic switching devices can be utilized in a medium voltage converter, the low voltage IGBTs in this application are capable of much higher switching frequencies when compared to their high voltage counterparts. This means that individual IGBTs are capable of switching speeds of over 2 kHz provided there is sufficient thermal management with respect to the switching losses and conduction losses. This is where the true advantage of the SCHB topology, coupled with PSCPWM, can begin to be realized with respect to the harmonic content of the output waveform. Equation 4.4 governs the center point of the first noise mode generated on the phase voltage output [35].

\[
F_\theta = 2KF_S : K = \text{Number of Series Connected Bridges}
\]

With this application having four series connected H-bridges, the first noise mode is centered around 8 times the switching frequency of the individual H-bridges and additional side band cancelation is provided when observing the phase to phase voltages [35]. Figure 4.7
demonstrates the harmonic spectrum of the phase voltage output of the SCHB topology with an assumed switching frequency of 2 kHz. The first noise mode is centered on 16 kHz and subsequent higher order noise modes are at multiples of the first mode. Since the harmonic spectrum is so low prior to the first noise mode, Figure 4.7 uses the log base 10 of magnitude in the lower trace.

Figure 4.7: The phase output voltage frequency spectrum given an individual H-bridge switching frequency of 2 kHz and a 60 Hz modulation index of 0.75. The first noise mode is centered around 16 kHz, which is eight times the individual H-bridge switching frequency.

Another ancillary benefit of utilizing PSCPWM is with respect to the overvoltage capabilities. As all of the individual H-bridges are continuously switched by the carrier waveforms, load is balanced closely between each of the H-bridges and the overvoltage is continuously online. Thus, the modulation index of the waveforms is based upon the full scale voltage of all four H-bridges connected in series and the modulation index of nearly 0.75 is required for the nominal output voltage of 4.16 kV.
Focusing back on the active front end of the SCHB topology for this application, some complexities are introduced by the mutual coupling between the three active front ends connected in parallel on the three secondary windings. For the purposes of this research, these complexities will be neglected and a simplified decoupled, active front end model will be utilized. This simplified decoupled model will assume that each active front end is connected to the point of common coupling with the utility connection through its own linear inductance and not through multi-winding transformer.

However, both the mutually coupled and the simplified decoupled models rely on voltage oriented control for voltage regulation of the DC bus voltage. As shown in Figure 4.8, the fundamental foundation of voltage oriented control of a three phase, active front end is very similar to the operation of a synchronous machine, albeit in a completely different dynamic manner. The simplified explanation of voltage oriented control is that the active front end is able to control the excitation voltage, E, such that the current drawn from the voltage source results in the commanded power flow through the linear inductance and the commanded power flow is determined by the voltage error of the DC bus. If the DC bus voltage is low, active power is drawn from the utility source and if the DC bus voltage is high, active power is delivered to the utility source.
Figure 4.8: The simple circuit schematic of voltage oriented control of an active front end. The excitation voltage is controlled by the PWM converter such that the desired power is drawn from the voltage source through the isolation impedance.

Inherently, the complete voltage oriented controller is more complex than this, as is demonstrated by the block diagram in Figure 4.9. The design of the active front end voltage oriented control utilized in this research is modeled after the work found in [36] and [37] where the design of the active front end control is applied three wire power converter applications. However, the application of the voltage oriented control differs in one significant way when applied to the SCHB topology.

Figure 4.9: The block diagram of the voltage oriented control consisting of the DC bus voltage regulator and decoupled DQ current regulators, with the final output being the excitation voltage of the active front end.
Being that the SCHB topology consists of three phase active front ends and single phase output H-bridges, there exists considerably more DC bus voltage ripple due to the single phase output H-bridges than if the output was a balanced three phase motor drive. This DC bus voltage ripple cannot practically be eliminated or regulated. For this application, a notch filter is added to the feedback of the measured DC bus voltage in order to remove this ripple from the error calculation. By adding the notch filter, the bandwidth of active front end is only marginally impacted and yields much better regulation results compared to restricting the bandwidth below the DC bus ripple frequency. One of the contributing factors to the output current overload capabilities is the DC bus voltage limits, which are plus or minus 200 VDC of the regulated DC bus voltage, equal to a range from 900 VDC to 1300 VDC.

The fundamental components of the physical implementation of the power amplifier have been presented but to achieve real-time performance of the model, some additional approximations will be required. The primary challenge is that the physical system contains a large number of parallel components to achieve the power ratings required and when modeling, these parallel components will need to be combined into a single equivalent model of the system. This includes the active front ends, the DC buses, and the output H-bridge converters. The equivalent model of the SCHB topology will be simulated in real-time on a Real Time Digital Simulator. The equivalent model detail will be discussed in Chapter Seven.
Step-Up Transformers

As indicated by Figure 4.5, the voltage step-up transformers that connect the variable voltage source to the reactive divider network are separated into two 7.5 MVA transformers. The operational requirements of these transformers to meet the objectives of the Hybrid Method include: both 50 and 60 Hz operation, the capability to withstand 133% continuous overvoltage, and be able to pass a zero sequence voltage of at least 33% of the rated nominal voltage. Each of these requirements impacts the design and manufacturability of these transformers.

Focusing on the operational requirement that the transformers must be able to pass zero sequence voltage, the possible transformer designs are limited because the standard three limb core type delta to wye transformer for distribution applications does not meet this requirement. Noting that the delta winding imposes a shunt zero sequence impedance in parallel with the magnetizing branch, this transformer cannot effectively pass zero sequence voltage. Even if a wye-wye winding configuration were used, there exists no zero sequence flux path other than through the tank [29]. This would result in excessively high magnetizing current requirements as the transformer would attempt to magnetize the zero sequence voltage through paths outside of the core. Instead, there are two rather common transformer designs that are capable of passing zero sequence voltage with nominal magnetizing currents, namely a bank of three single phase transformers or one three-phase, five limb core type transformer. These two transformer designs are shown in Figure 4.10.

The five limb core type transformer allows for the zero sequence capability by having two outer limbs that do not contain windings and offer a low reluctance path to zero sequence flux. These outer limbs are typically designed to have 50% of the cross-sectional area of the
limbs with windings such that the addition of the two outer limbs is equivalent to the cross sectional area of one of the inner limbs. Given this typical ratio of cross-sectional area, the zero sequence voltage capabilities of the five limb core type transformer are typically 50% of the rated nominal voltage. However, one major drawback to the five limb core is that the residual flux within the outer limbs is not known under nominal positive sequence voltage conditions and the arbitrary injection of zero sequence voltage could result in saturation of the outer limbs due to the remnant magnetic field.

Figure 4.10: The physical structures (a) and (c) and three phase schematics (b) and (d) of the two possible transformer configurations that allow for the passage of zero sequence current and voltage.
In contrast, the use of three single-phase core type transformers directly eliminates the application of sequence components as the three single-phase transformers are completely independent. Thus, when in operation with the respect to the Hybrid Method, there exists no coupling between phases which would result in a complex control algorithm and the flux within the transformers needs to be managed only on a per phase basis. Simply, for comparison purposes, this transformer configuration is able to pass zero sequence voltage equal to nominal rated voltage. The use of three single-phase transformers connected in a wye-wye configuration is the transformer configuration of choice with respect to the practical implementation of the Hybrid Method.

The additional two operation requirements of the transformer, 50 and 60 Hz operation and 133% continuous overvoltage, ensure that the resulting transformer is rather robust with respect to magnetic saturation. Since the transformer is to operate at both 50 and 60 Hz, the flux within in the core when operating at 60 Hz is approximately five-sixths of the flux when operating at 50 Hz given the same applied voltage. Adding to the robustness is the fact that the transformer is being designed for continuous overvoltage capabilities, meaning that the nominal flux within the transformer given nominal voltage is well below the saturation region of the core. To allow for even more voltage adjustment, the transformers are equipped with two, +5% and two, -5% high voltage winding taps with a no load tap changer, allowing for high voltage winding to be adjusted +/- 10% of the rated nominal voltage. Using these criteria of the transformer design, Figure 4.11 demonstrates the rated continuous power of the amplifier when connected to the transformers. It is assumed that the nominal 50 Hz voltage is 22 kV and that the nominal 60 Hz voltage is 24 kV.
This section only briefly discusses the physical construction of the transformer and the turns ratio of the transformers. More detail on the modeling of the flux within the transformer will be discussed in Chapter Seven. A parallel equivalent model will be used to match the equivalent model of the power amplifier. Even with the additional ‘head room’ with respect to magnetic saturation of the transformer under nominal operating conditions, it is imperative that the voltage transitions produced by the variable voltage source be controlled in such a fashion that the dynamic range of the variable voltage source is preserved without magnetic saturation.
Reactive Divider Network

This section will discuss the practical implementation of the Reactive Divider Network (RDN) of the Hybrid Method shown in Figure 3.5 and discussed in Chapter Three. The primary focus of this section is how discretely variable impedances can be created by the reactive divider with a minimum amount of components while maintaining a high degree of flexibility. From the previously discussed ratings of the Hybrid Method and the desired discrete incremental step sizes of the inductance, a novel circuit will be developed to achieve these objectives through the usage of two tapping methods. It should be reiterated that the inductors used for this type of application must be of an air core inductor design in order to achieve the linear responses regardless of the fault current magnitude.

The nominal power rating of the Hybrid Method demonstrated in this section is 15 MVA at 23.9 kV. This yields a base impedance of roughly 38 ohms and a base inductance of roughly 100 mH at 60 Hz. Given that it is desired to have discretely incremental step sizes of 5% of the rated impedance, inductive step sizes of 5 mH are needed. For the maximum series resistance to achieve a time constant of one fundamental period at 60 Hz, a maximum series resistance of approximately 6 ohms would be required. However, this would assume lossless inductances and, if we assume a quality factor of 40, the maximum series resistance required would be less than 5 ohms. For reasons that will be obvious later in this section, a maximum series resistance of 5 ohms is selected.

Figure 4.12 demonstrates the single phase representation of a novel circuit that is capable of creating the above specified discretely stepped impedances with an extremely high degree of flexibility. In order to achieve this, there are two methods of tapping used within the circuit.
The first method is to use six position tapped impedances and a no-load radial disk tap changer to select between the six positions to create the discretely variable impedance. With the desired inductive step size of 5 mH, a six tap 25 mH inductor can be used to achieve step changes from zero to 25 mH in 5 mH increments. Since the maximum series resistance is 5 ohms, the same type of six position tap switch can be used with five 1 ohm resistors in order to achieve a variable discrete resistance from zero to 5 ohms in 1 ohm increments. The second method of tapping utilized in the reactive divider network uses medium voltage circuit breakers that switch larger (25 mH) fixed inductors into and out of the circuit. Since the total inductance of the fixed and tapped inductors is the same, the same inductor design can be used for both.

Coupling these two tapping methods together in Figure 4.12, the discretely variable resistance is connected to a discretely variable inductance to formulate the basis of the series impedance. Another discretely variable inductance is used to formulate the basis of the shunt impedance. Connected in series with these two sets of impedances are three fixed inductors. The series connection points of the three inductances are connected to the point of common coupling with the device under test through four medium voltage vacuum breakers, designated as LDRT 1 – 4. This allows for the vacuum breakers to either insert or remove the fixed inductors with respect to the total series or shunt impedance. Additionally, the complete reactive divider network can be bypassed and isolated by closing the circuit breaker designated as LDFM and by opening LD-RDN1 and LD-RDN2.
Figure 4.12: The simplified single phase diagram of the Reactive Divider Network detailing the interconnection with the power amplifier and point of common coupling.

Table 4.3 demonstrates the various options available with the novel reactive divider network circuit. The left column identifies the on or off state of the four LDRT switches. The results are not a direct binary count of the switch states due to several redundant or invalid state combinations. Given the flexibility demonstrated, there are over 300 possible series and shunt inductance combinations for this circuit.
Table 4.3: Reactive Divider Network Inductance Tap Options

<table>
<thead>
<tr>
<th>Fixed Switch Positions (1-2-3-4)</th>
<th>Shunt Fixed (mH)</th>
<th>Shunt Variable (mH)</th>
<th>Series Fixed (mH)</th>
<th>Series Variable (mH)</th>
<th>Total Shunt (mH)</th>
<th>Total Series (mH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1-1-0</td>
<td>0</td>
<td>0-25</td>
<td>25</td>
<td>0-25</td>
<td>0-25</td>
<td>25-50</td>
</tr>
<tr>
<td>1-1-0-0</td>
<td>0</td>
<td>0-25</td>
<td>50</td>
<td>0-25</td>
<td>0-25</td>
<td>50-75</td>
</tr>
<tr>
<td>1-0-0-0</td>
<td>0</td>
<td>0-25</td>
<td>75</td>
<td>0-25</td>
<td>0-25</td>
<td>75-100</td>
</tr>
<tr>
<td>0-1-1-1</td>
<td>25</td>
<td>0-25</td>
<td>0</td>
<td>0-25</td>
<td>25-50</td>
<td>0-25</td>
</tr>
<tr>
<td>0-1-1-0</td>
<td>25</td>
<td>0-25</td>
<td>25</td>
<td>0-25</td>
<td>25-50</td>
<td>25-50</td>
</tr>
<tr>
<td>0-1-0-0</td>
<td>25</td>
<td>0-25</td>
<td>50</td>
<td>0-25</td>
<td>25-50</td>
<td>50-75</td>
</tr>
<tr>
<td>0-0-1-1</td>
<td>50</td>
<td>0-25</td>
<td>0</td>
<td>0-25</td>
<td>50-75</td>
<td>0-25</td>
</tr>
<tr>
<td>0-0-1-0</td>
<td>50</td>
<td>0-25</td>
<td>25</td>
<td>0-25</td>
<td>50-75</td>
<td>25-50</td>
</tr>
<tr>
<td>0-0-0-1</td>
<td>75</td>
<td>0-25</td>
<td>0</td>
<td>0-25</td>
<td>75-100</td>
<td>0-25</td>
</tr>
</tbody>
</table>

Having evaluated the reactive divider network on a single phase basis, Figure 4.13 demonstrates the three phase reactive divider network. In the three phase system, each phase is controlled independently. This means that the series bypass switches, series impedances, shunt impedances and shunt fault switches are all completely independent from each other. This results in an extremely high degree of flexibility and fine tuning capabilities of this implementation of the Hybrid Method. Perhaps the only item missing from this implementation is a discretely variable shunt resistance but, that can be easily added to the circuit if desired. Also depicted in Figure 4.13 is the neutral bonding shunt switch to the left of the shunt fault SCR switches. This switch is what is used to tie the common shunt fault switch point to ground if required by the fault type. Additionally, with some modifications to this connection point, more complex faults such as a concurrent line to ground and line to line fault could be created if needed.
Figure 4.13: The complete three phase schematic of the Reactive Divider Network with independent phase operation of the series bypass switches, the series impedances, the shunt impedances and the shunt fault switches.

The final element of the reactive divider network that is essential to the performance of the Hybrid Method is the use of solid-state power electronic switches for both the series bypass switches and the shunt fault switches. As is typical with most medium voltage solid-state switch applications, such as those employed in Static VAR Compensators (SVCs), the switch consists of anti-parallel thyristors connected in series to obtain the blocking voltage required. General high voltage, phase controlled thyristors lend themselves well to this particular application because they have a natural current extinction near zero-crossings, extremely high short term current overload capabilities, and very precise point-in-wave turn-on characteristics when compared to a circuit breaker. Additionally, the blocking voltage of the high voltage thyristors is easily in the 4 kV to 8 kV range with forward current ratings in the 200A to 800 A range. Figure 4.14 demonstrates the implementation for this specific application, where the individual thyristors are rated for 6 kV forward blocking voltage and 500 A continuous forward conducting current.
Some special considerations are required for this particular application. These include the application of RC snubber circuits to slow the voltage rise across the devices when they turn off due to the instantaneous voltage rise associated with switching inductive circuits and the fact that the complete solid-state AC switch should be rated for the line to line voltage with an additional safety margin. The application of the RC snubber circuit impacts several aspects of the complete hardware design because of the cable capacitances, the inductive nature of the complete circuit, and the harmonic content associated with both the variable voltage source and the device under test. These contributing factors will result in series and parallel resonances within the reactive divider network, however, this is outside of the scope of this research and will be relegated as future work.

Nevertheless, the switch must be rated for line to line voltage because, with a line to line fault scenario, two switches are connected in series but there exists some uncertainty that both switches will turn off at the same time. Thus, the prudent design practice is to ensure that a single switch is capable of blocking the complete line to line voltage, including the possible overvoltage margins of the system, in case one of the switches is unable to commutate off.
While the implementation of a medium voltage, solid-state AC switch includes a multiple of power electronic switching devices, when attempting to simulate these in real-time on the Real Time Digital Simulator, an equivalent model must be utilized. Within this equivalent model the complete solid-state AC switch is to be modeled as a single anti-parallel thyristor pair and some concessions must be made with respect to the voltage rise across the individual devices. It is proposed that the most suitable model is to have the series equivalent RC snubber circuit in parallel with the anti-parallel thyristor set and neglect the impact upon individual devices. Clearly this will dramatically change the characteristics of the inner components of the actual system but, with respect to modeling, the values will be consistent. More detail on this effort will be given when the modeling of the switches within the Real Time Digital Simulator is presented in Chapter Seven.
CHAPTER FIVE
INVESTIGATIONS INTO METHODS OF TRANSFORMER FLUX MANAGEMENT

The enabling technology and novel research behind making the Hybrid Method a viable solution for fault ride-through evaluations is presented in this chapter. This novel research for implementation of the Hybrid Method entails the development of passive methods for managing the flux within the transformer such that fast voltage transitions can be achieved by the vector control system and the variable voltage source while avoiding magnetic saturation within the transformer core that couples the variable voltage source to the reactive divider network. For the purposes of this document, these methods will be introduced and described with respect to the Hybrid Method vector control system. Nevertheless, this research has the potential for much broader applications, including flux management in grid connected power electronic converters and dynamic response capabilities in microgrid applications that involve the use of transformers.

The purpose of this research is to determine a method(s) of tracking a reference voltage such that the integral of the tracking signal remains bounded within nominal limits and thus the flux in the transformer will also remain bounded. Clearly, to meet the performance requirements of the Hybrid Method, the time for convergence of such a filter needs to be on the order one period of the fundamental frequency or less. However, it should be noted that there are theoretical limitations on how fast a passive tracking method can converge given a disturbance in the reference signal. Inherently, active methods of injecting additional voltage to counter the magnetization flux can be implemented at the possible sacrifice of power quality disturbances being imposed upon the voltage at the point of common coupling.

The three methods that will be outlined below are referred to as passive because they do not actively compensate the integral of the voltage by calculating and injecting inverse voltage
during reference voltage transitions. Instead, the passive filters simply ensure tracking of the voltage reference in such a manner that the integral of the filter output is bounded during and after any reference voltage transitions. The focus of this research also involves methods of constraining the tracking of the reference voltage to only the fundamental frequency, which is the basis of the vector control strategy for the Hybrid Method. This research has yielded three different methods for bounding the flux during voltage transitions, each with their own unique properties.

The first method evaluated is a simple linear interpolation between the two fixed vector representations of a sinusoidal signal over an integer number of fundamental periods. Equation 5.1 demonstrates this linear interpolation. It can be easily proven that, with a transition time of one period, the integral over the period of transition is equal but opposite of the initial condition. Given an integration period of one fundamental period, the output voltage will converge to the input voltage in exactly one period of the fundamental. The disadvantages to this method are that the initial and final sinusoidal functions must be known a priori to any reference transition and both functions are required to be constrained to the fundamental frequency before application of this method.

\[ V(t) = V_{\text{init}}(t) + (V_{\text{init}}(t) - V_{\text{final}}(t)) \left( \frac{t - t_0}{\tau} \right) (u(t - t_0) - u(t - \tau)) + u(\tau) \]

5.1

\[ \text{for } \tau = \frac{1,2,...}{2\pi\omega} \]

While this method of linear interpolation easily demonstrates the functionality of a passive method, it lacks the ability to track a sinusoidal reference voltage that continuously changes in magnitude and phase and imposes implementation challenges with respect to a vector control algorithm. Additionally, the method relies on attenuation of signals outside of the
fundamental frequency to be provided by external filtering because the initial and final functions must be constrained to the fundamental frequency for proper operation of the method.

The next two methods are based upon implementations that have the characteristics of offering continuous reference voltage tracking and attenuation to higher order harmonics while still ensuring the integral of the output voltage remains bounded. The characteristic of continuous reference voltage tracking is required for successful implementation into a vector control system where the reference signal will need to respond to known and unknown dynamic conditions.

The second method investigated is built around a band-pass filter transfer function that is often referred to in the literature as a Second Order Generalized Integrator (SOGI) [38], [39], [40]. The SOGI has generally been applied as a successor to proportional resonant control as it offers unity gain at the band pass frequency and sufficient out of band attenuation. The SOGI filter is found in applications pertaining to power electronic converters in the research areas of single-phase, phase-lock-loops [41], harmonic separation for active filtering applications [42], and three-phase power electronic converter control systems designed to operate under severe unbalance [43]. However, the literature to this point has not clearly articulated that this structure can be utilized for an application such as this, where the memory of the past signal states is of importance in order to ensure a bounded integral.

This second order structure offers an attenuation of -20 dB per decade above and below the pass band, which is centered on the fundamental frequency. The SOGI filter also yields unity gain at the fundamental frequency while allowing for adjustment to the damping factor by adjusting the gain. By letting the filter gain $k = \sqrt{2}$, the damping factor is equal to $1/\sqrt{2}$ which generally offers a good compromise between rise time and overshoot in second order systems.
This filtering method has an infinite impulse response (IIR) and is capable of achieving output convergence within typical engineering limits to abrupt changes in the reference voltage in less than one cycle. Figure 5.1 demonstrates the application of three independent SOGI filters in order to track the three phase voltages required for this application. The SOGI filters will be thoroughly discussed later in this chapter as it is the flux filtering method that will be utilized in the implementation of the Hybrid Method within this work.

![Diagram of SOGI filters](image)

Figure 5.1: The control block diagram of passive flux filter comprised of a second order generalized integrator (SOGI) to achieve FIR characteristics for tracking the individual phase voltages.

The third method is a novel implementation of a passive flux filter that is a composite algorithm developed around the use of rotational transformations and moving average filters for tracking the positive and negative sequence components while employing a SOGI filter for tracking of the zero sequence component. Figure 5.2 demonstrates the structure of what will be referred to as the composite DQ0 method. This method is capable of achieving faster
convergence with respect to the positive and negative sequence components and allows for the tracking of the positive, negative, and zero sequence symmetrical components through intermediate variables.

The fundamental foundation utilized in this composite method builds upon the basic characteristic of the synchronously rotating reference frame where negative sequence components are represented on the forward rotating reference frame as double frequency components. Utilizing a method that is increasingly being found in the literature [44], [45], [46], [47], two counter-rotating synchronous reference frames can be created to evaluate the positive and negative sequences separately. These rotating reference frames are not decoupled and the positive and negative sequence components are represented as double frequency components on the opposite rotational reference frame [48].

The flux filtering capabilities can be made possible by the novel application of memory in the filter, which is provided by moving averages of the direct and quadrature signals in both
the positive and negative rotating reference frames. Since a sine wave has an average value of zero over a single period, the moving averages have window lengths set to one half of the fundamental period in order to average out the double frequency component coupled from the counter rotating signal, be it positive or negative sequence. At the same time, this memory allows for the positive and negative sequence components to have an integral that is bounded once reconstructed into the phase quantities. This boundedness of the integral of the output signal is made possible by the exact same moving window integral that removes the double frequency components. The moving window integral forces the trajectory of the change in the fundamental component of the reference frame to traverse the complex rotating plane such that the integral of the resulting signal remains bounded. As this method is not utilized in the final design, these concepts are only discussed in this work and no formal proof is offered.

The reconstruction process is accomplished by referencing the positive sequence complex magnitude back to the forward rotating reference frame and the negative sequence complex magnitude back to a reference frame rotating at twice the speed of the backward reference frame. This composite method exhibits finite impulse response (FIR) characteristics with respect to the positive and negative sequence components but is still constrained by the IIR characteristics of the SOGI that must be applied for the zero sequence component. It should be observed that this method is only applicable to three-phase systems and does not eliminate the cross coupling between the sequence components.

To illustrate the performance of both the SOGI and the composite DQ0 methods of flux filtering, an example is given in Figure 5.3. In this example, the reference signal is rotated by 180°, or it can be viewed as an inversion of the magnitude, in order to demonstrate the tracking ability of both methods and their conversion times. The reference signal is changed at the worst
possible point-in-wave with respect to the integral of the output, a zero crossing of the reference waveform. The fundamental frequency of the reference voltage is set to 50 Hz in order to allow for straightforward cycle to time conversions.

Figure 5.3 includes the waveform plots demonstrating the tracking performance of each method, the integral of the tracking signal, and error between the reference and the tracking signal. From the waveforms, it is clear that both methods provide sufficient tracking performance while keeping the integral of the tracking signal bounded and symmetrical. The waveform depicting the error between the tracking signal and the reference signal shows that the composite DQ0 method achieves convergence within one half cycle of the fundamental period with no overshoot. Such performance is only achievable with FIR systems. However, it should be noted that this is only possible because the reference waveform contains only positive and negative sequence components and no zero sequence components are present to be subjected to the IIR response of the SOGI filter.
Figure 5.3: A demonstration of the flux filtering capabilities and a comparison of the response of the SOGI based flux filter and the DQ0 composite flux filter. The SOGI gains are set to \( k = \sqrt{2} \) for both methods. The top plot demonstrates both methods against the reference, where the reference is phase shifted by 180 degrees, the middle plot shows the integral of signals in the top plot, and the bottom shows the instantaneous error between the reference and tracking signal.

Even though the results demonstrated in Figure 5.3 indicate that the DQ0 composite method of flux filtering has some performance benefits over the SOGI implementation, these benefits only hold true for very specific three-phase signal relationships. On the other hand, because the SOGI implementation is completely phase independent, the control strategy can be implemented on a per phase basis. Additionally, with respect to implementation of the control, the SOGI filter represents a second order transfer function that is rather straightforward to adapt to and program into a digital signal processor. In the next sections, the characteristics of the
SOGI that pertain to implementation of the Hybrid Method will be explored with a heavy emphasis placed upon the integral of output signal given the characteristics of the input signal.

**Second Order Generalized Integrator Characteristics**

In this section, a single second order generalized integrator (SOGI) will be examined. The SOGI is a unity gain, zero phase, band-pass active filter structure that is able to be tuned to the fundamental frequency of a system. Figure 5.4 depicts the block diagram of the second order generalized integrator. One aspect of the SOGI filter that has found traction in single phase, phase lock loop applications is that the structure contains both direct and quadrature outputs as demonstrated in Figure 5.4 by $Y_d(s)$ and $Y_q(s)$, respectively. The transfer functions of the direct and quadrature outputs can be found in equations 5.2 and 5.3, respectively. For the purposes of this chapter, we will assume that the fundamental frequency of the system is 60 Hz.

![Figure 5.4: The block diagram of the Second Order Generalized Integrator (SOGI) demonstrating the direct, $Y_d(s)$, and quadrature, $Y_q(s)$, outputs.](image)

$$H_d(s) = \frac{Y_d(s)}{R(s)} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \quad 5.2$$
Figure 5.5 and Figure 5.6 demonstrate the Bode plots of the direct output and quadrature output, respectively. As can be seen with the transfer functions and the Bode plots for the SOGI, the direct and quadrature outputs have different frequency response characteristics due to the location of the zeros in the numerator. As the quadrature output does not contain a first order zero at the origin, the quadrature output will not exhibit good flux filtering capabilities. Thus, for the remainder of this chapter, the characteristics of the direct output will only be considered when referring to the SOGI filter.

Figure 5.5: The Bode plots of the direct output of the SOGI filter for varying gains.
The Bode plots of the quadrature output of the SOGI filter for varying gains. Given the second order nature of the transfer function the nominal gain for the SOGI filter is chosen as the square root of 2 in order to make the damping factor of the second order system equal to one divided by the square root of 2. This is a commonly chosen damping factor in second order systems due to the acceptable compromise between rise time and overshoot in the system. The varying gains of the SOGI filter used in this section are one half and twice the nominal gain to demonstrate the response of the SOGI to these alternative gains.

Figure 5.7 demonstrates the step response of the SOGI filter given varying gains for the filter and confirms that the nominal gain results in a good compromise between the initial step response transient and the settling time of the system. Figure 5.8 demonstrates the linear time domain responses of the SOGI filter to an input waveform that is inverted after two cycles. This figure not only shows the windup time associated with a flat start of the SOGI filter but also the dynamic tracking capabilities that will be utilized in this application.
Figure 5.7: The step response of the direct output of a SOGI given varying gains.

Figure 5.8: The linear time domain responses of the direct output of a SOGI for varying gains given a step change of negative one on the input signal.

More pertinent to this application, however, is the time domain response of the integral of the output of the SOGI filter. Due to the direct output of the SOGI filter containing only one zero and this zero is at the origin, it can be observed that the transfer function of the normalized integral of the direct output should, and does, result in the transfer function of the quadrature
Equations 5.4 and 5.5 are used to calculate the normalized integral of the SOGI filter output. The normalized integral consists of multiplying by the resultant by the fundamental frequency such that time domain results can be compared directly on a normalized basis.

\[ \Phi_{\text{Norm}}(t) = \omega \Phi(t) = \omega \int H(s)dt \quad \text{(5.4)} \]

\[ \Phi_{\text{Norm}}(t) = \omega \int H(s)dt = \left( \frac{\omega}{s} \right) \left( \frac{k\omega s}{s^2 + k\omega + \omega^2} \right) = \frac{k\omega^2 s}{s(s^2 + k\omega + \omega^2)} \quad \text{(5.5)} \]

Figure 5.9 demonstrates the Bode plots for the normalized integral of the SOGI direct output given varying gains. From these Bode plots, it is apparent that the boundedness of the normalized integral is guaranteed for all input frequencies. However, for frequencies below the fundamental, the gain of the normalized integral of the SOGI filter can be greater than unity. Equation 5.6 illustrates that the DC gain of the normalized integral of the SOGI filter is simply equal to the gain of the SOGI filter.

Figure 5.9: The Bode plots for the normalized integral of the direct output of the SOGI for various gains.
While the fact that the DC gain of the normalized integral of the SOGI filter is not problematic of the signal contains only frequency components greater than or equal to the fundamental component, it can have a significant impact if the signal contains low frequency components. Figure 5.10 demonstrate the linear time domain response of the normalized integral of the SOGI filter given the exact same conditions as Figure 5.8. Here the response of the normalized integral to the inverted fundamental frequency input is clearly bounded. More importantly, the integral remains generally symmetrical about the axis, with only small transient deviations for SOGI filter gains greater than one.

Figure 5.10: The linear time domain responses of the normalized integral of the direct output of a SOGI for varying gains given a step change of negative one on the input signal.

The analysis up until this point demonstrates that the SOGI filter is a perfect candidate for providing the flux filter of the feed-forward reference voltage control and will in fact be used for the feed-forward reference voltage control loop. However, knowing that the normalized
integral of the SOGI filter has a non-zero DC gain, it is not directly applicable to the feed-back
loop where the inputs are the asymmetrical fault currents of the device under test. Even though
the normalized integral is bounded for such asymmetrical inputs, it is not symmetrical about the
axis, and this can result in magnetic saturation of the transformer. To illustrate this, Figure 5.11
and Figure 5.12 demonstrate the linear time domain responses to an input signal that contains a
unity rectangular DC offset function for the SOGI filter and the normalized integral of the SOGI
filter, respectively. Also included in Figure 5.12 is a plot of normalized integral of the input
waveform to demonstrate exactly how the single SOGI filter helps to bound the flux within the
transformer.

Figure 5.11: The linear time domain responses of the direct output of a SOGI for varying gains
given a step change with a DC offset on the input signal.
Cascaded Second Order Generalized Integrators Characteristics

As described in the previous section, in order to overcome the inherent issue of the normalized integral of the SOGI filter containing a DC gain, this section will examine utilizing two cascaded SOGI filters. Figure 5.13 illustrates the block diagram of two cascaded SOGI filters where the direct output of the first filter is connected to the input of the second filter and the direct output of the second filter is the cascaded filter output. By cascading the two filters the desirable properties of the single SOGI filter, unity gain, and zero phase shift, are retained. Figure 5.14 demonstrates the Bode plots of the cascaded SOGI filters for varying gains.
Figure 5.13: Block diagram of two cascaded SOGI filters.

Figure 5.14: The Bode plots for cascaded SOGI direct outputs given various gains.

The Bode plots of the cascaded SOGI filters appear similar to those for a single SOGI filter except for the fact that the pass band is wider and the phase angles traverse a range of 360° instead of just 180°. As one would expect, cascading the SOGI filters results in slower step responses, as demonstrated in Figure 5.15, where the step responses of the single filters and cascaded filters are compared for the same gains. As with just the single filter, the cascaded filters with nominal gain show the best compromise in performance between the initial transient step response and the settling time.
Figure 5.15: The step response for cascaded SOGI direct outputs given various gains.

With respect to evaluating the normalized integral of the two cascaded SOGI filters in equations 5.7 and 5.8, it is clear that the additional zero at the origin, provided by the second SOGI filter, will result in a zero DC gain as evident in equation 5.9. Figure 5.16 demonstrates the Bode plot of the transfer function of the normalized integral of the cascaded SOGI filters.

\[
\Phi_{Norm}(t) = \omega \int H^2(s) \, dt = \omega \int H(s)H(s) \, dt
\]

5.7

\[
\Phi_{Norm}(t) = \left( \frac{\omega}{s} \right) \left( \frac{k\omega s}{s^2 + k\omega s + \omega^2} \right)^2 = \frac{k^2 \omega^3 s^2}{s(s^2 + k\omega s + \omega^2)^2}
\]

5.8

\[
\lim_{s \to 0} \omega \int H^2(s) \, dt = \frac{0}{\omega^4} = 0
\]

5.9
Figure 5.16: The Bode plots for the normalized integral of cascaded SOGI direct outputs given various gains.

It can be observed that, by cascading two of the SOGI filters, a low band attenuation of -20 dB per decade can be preserved in the integral and thus the response of the integral to DC offsets should now be symmetrical about the axis. Figure 5.17 and Figure 5.18 demonstrate the linear time domain responses of the cascaded SOGI filters and the normalized integral of the cascaded SOGI filters, respectively, to an input signal that contains unity DC offset rectangular function. This is the exact same scenario from the previous section demonstrating that the cascaded SOGI filters do a good job of tracking the input signal while ensuring that the integral of the output signal remains centered on the axis. With respect to the implementation of the Hybrid Method, the utilization of two cascaded SOGI filters in the feedback compensation voltage loop will achieve the flux filtering performance required and will be utilized in the next chapter to implement the vector control strategy.
Figure 5.17: The linear time domain responses of the cascaded direct outputs of the SOGI given varying gains.

Figure 5.18: The linear time domain responses of the normalized integral of cascaded SOGIs given various gains with a step response with a DC offset.
The final figure in this section, Figure 5.19, demonstrates the tracking performance of a single SOGI filter with two cascaded SOGI filters for the nominal gain with a rectangular DC offset step response. It can be ascertained that the single SOGI filter achieves faster settling times with respect to the step responses but the two cascaded SOGI filters have much less overshoot. These properties will play into the final implementation of the vector control strategy in the next chapter.

Figure 5.19: The linear time domain responses for comparison of a single SOGI versus two cascaded SOGIs for a step response with a DC offset.
CHAPTER SIX
VECTOR CONTROL IMPLEMENTATION METHODOLOGY

This chapter will discuss the implementation of the vector control system for controlling the dynamic behavior of the variable voltage source in the Hybrid Method when performing fault ride-through evaluations. This chapter discusses the details associated with both the feedforward reference voltage control and the feedback voltage compensation control along with their associated switch timing and logic. The switch timing and logic is instrumental in controlling the switch states of the system and the subsequent voltage compensation and voltage reference transitions in order to control the transient nature of the system. The overall operation of the Hybrid Method is governed by a simple state machine.

Figure 6.1: The block diagram demonstrating the main control elements and how they communicate with the Hybrid Method physical system.
Feed-Forward Reference Voltage Control

The implementation of the feed-forward reference voltage control is fairly straightforward. The voltage reference provided by this control is the sole reference of the system for which a device under test must synchronize with in order to deliver or absorb power. The basis of the feed-forward reference voltage control is the creation of quadrature reference sinusoidal waveforms, a cosine and a sine wave, at the fundamental frequency that are not altered in any way during the operation of the vector control system. Instead, these reference waveforms will be used as the basis for the complex vector rotation.

Equation 6.1 demonstrates the feed-forward reference voltage calculation where \( V_\alpha(t) \) and \( V_\beta(t) \) represent the real and imaginary time domain components of complex scalar vector \( K(j\omega,t) \). Figure 6.2 illustrates the block diagram of the complete feed-forward reference voltage calculation where the output of the complex vector calculation is fed into a SOGI filter in order to ensure that transitions in the reference vector do not result in magnetic saturation.

\[
V_{REF}(t) = V_\alpha(t) \cos(\omega t) + V_\beta(t) \sin(\omega t) \quad 6.1
\]

Figure 6.2: The block diagram of the feed-forward voltage reference control loop.
**Feed-Forward Reference Voltage Shunt Switch and Transition Control**

The logic and timing associated with the shunt fault switches and the transitions in the complex reference vector calculation are constrained in this dissertation to operating simultaneously on all three phases since all three phases use the same timing control. However, because the calculations and switching logic parameters are controlled on a per phase basis, this does not imply that all three phases must be switched, nor that all three complex reference vectors are affected by the control algorithm. Figure 6.3 illustrates the signal logic and timing associated with the feed-forward reference voltage control. In the controller implementation, all of the variables associated with the logic are parameterized in the control algorithm.

**Figure 6.3:** The single phase representation of the timing and logic for the shunt fault switches. The rectangular traces indicate digital logic of the signals and the switch states.

In Figure 6.3 there are two distinct waveforms – the underlying sinusoidal reference voltage waveform and a saw tooth waveform that represents an angular calculation obtained from the underlying sinusoidal reference waveform. Additionally, there are three states used within the control logic: Arm Switch, Switch Voltage Reference, and Switch Pulse. The arm
switch state is used to indicate that the state of the shunt fault switches is desired to be changed by the master state machine controller and is the only input to the shunt switch logic.

When the arm switch state goes high, the logic waits for the appropriate angle, Angle On, in which to transition the voltage reference. Since the reference voltage is fed through the SOGI filter, the rise time seen in the previous chapter is roughly one half cycle of the fundamental period. Thus, the transition in the reference is begun prior to actually closing the shunt fault switch to ensure some overlap. The control logic then waits for the appropriate angle, Angle Fire, before actually sending the firing pulse to the shunt fault switch. Since the physical implementation of the shunt fault switch is a solid-state thyristor based AC switch which supports random turn on, the physical state of the switch (switch action) rises at the same time. It should be noted that the firing angle of the switch directly controls the point-in-wave of the fault initialization.

When the arm switch state goes low, the control logic waits for the appropriate angle, Angle OFF, before removing the firing pulse from the switch. The control logic then waits a full half cycle before resetting the Switch Voltage Reference state. Thus, the switches are allowed the proper time associated with sequentially clearing the fault at the zero crossings of the fault current prior to the voltage being returned to the nominal reference voltage.

**Feedback Compensation Voltage Control**

The implementation of the feedback compensation voltage control is more complex than that of the feed-forward reference voltage control. This section will discuss how the feedback compensation voltage control is designed in order to take the measured output currents of the
device under test, convert them into compensating voltages, enforce an absolute maximum voltage magnitude through saturation, and constrain the final output to the fundamental frequency. All the while, the feedback compensation voltage control must ensure that the integral of the compensating voltages is bounded and symmetrical about the axis. Figure 6.4 illustrates the block diagram of the complete feedback compensation voltage control. This section will break apart the control into segments based upon their functionality and provide the reasoning behind their implementation with respect to the complete control loop.

The first section includes the input of the current measurements, a SOGI based pre-filter, and the series impedance voltage drop calculation. The second section involves the magnitude saturation of the calculated voltage drop, a SOGI based post-filter and an Nth order harmonic filter, also based upon SOGI filters.

Figure 6.4: The complete block diagram of the feedback compensating voltage loop in which the measured current is first pre-filtered, then the series impedance voltage drop is calculated and subjected to saturation limits.

Figure 6.5 demonstrates the first functional section of the feedback compensation voltage control. The function of the SOGI based pre-filter is to provide attenuation of harmonics outside of the fundamental frequency band, especially the very low frequency content associated with
asymmetrical fault currents. Thus, the voltage calculation can be applied to a more symmetrical waveform and the subsequent magnitude saturation will not be asymmetrical in nature.

\[ I_{OM}(t) \xrightarrow{\frac{k_p \omega_p s}{s^2 + k_p \omega_p s + \omega^2}} \frac{sX}{\omega} \xrightarrow{R + \frac{sX}{\omega}} V_C(t) \]

Pre-Filter 
Series Impedance Voltage Drop Calculation

Figure 6.5: The block diagram of the pre-filter and the series impedance voltage drop calculation.

If it is assumed that the pre-filter has removed most of the out of band harmonic content, the series impedance voltage drop calculation predominantly acts upon the fundamental frequency component and complex vector multiplication can be utilized. Given a single frequency sinusoidal waveform, the complex vector multiplication requires a direct, in phase, component and a quadrature, orthogonal phase component. Knowing that the series impedance is resistive and inductive, the desired quadrature signal should inherently lead the direct output because the voltage across an inductance leads the current. With respect to the voltage drop calculation, the resistive voltage drop is then a multiple of the direct signal and the inductive voltage drop is a multiple of the quadrature signal.

Due to the signal being predominantly sinusoidal, the quadrature component can be achieved by either taking the derivative of the direct signal or by taking the inverse of the integral of the direct signal. Noting that both of these methods of creating a quadrature component will result in non-uniform frequency domain characteristics, it can be observed that the resistive and inductive voltage drop calculations will not have the same frequency domain characteristics.
Both the derivative and integral methods of creating a quadrature component have been investigated. With respect to the frequency domain characteristics, the integral method will result in attenuation of higher order harmonics at the sacrifice of amplifying lower order harmonics. Conversely, the derivative method will result in the attenuation of lower order harmonics with the sacrifice of amplifying the higher order harmonics. To evaluate the differences between the two methods when coupled to the pre-filter, Figure 6.6 shows the Bode plots for both the derivative and integral methods with the pre-filter. It is clear that, when coupled to the SOGI pre-filter, the amplification in both methods is canceled by the attenuation of the SOGI filter and is limited to the SOGI gain – the square root of two in this instance. Additionally, the attenuation offered by each method is coupled with the out of band attenuation of the SOGI to result in a total attenuation of -40 dB per decade.

![Bode Plots of the Pre-Filter with Both Reactive Voltage Calculation Methods](image)

Figure 6.6: The Bode plots for utilizing a discrete difference method and a trapezoidal integration method of calculating the reactive voltage drop.
While the above discussion focuses on the analysis of continuous transfer functions, there are practical issues that must be addressed when implementing both methods into the feedback compensation voltage control. Figure 6.7 demonstrates the discrete time implementation of both methods with respect to the total complex vector voltage drop calculation. The integral method is implemented with a discrete time trapezoidal integrator and the differential method is implemented with a first order discrete difference. With respect to computation resources, neither method is excessively taxing in regards to implementation on a digital signal.

**Figure 6.7:** The block diagrams for the two methods of calculating the reactive portion of the series impedance voltage drop, (a) uses discrete trapezoidal integration and (b) uses a first order discrete difference.

There is one fundamental difference between both methods that is not demonstrated in Figure 6.7. That is the fact that the integral method is highly sensitive to the initial conditions while the derivative method is not. To overcome the sensitivity to the initial conditions, losses are commonly added to the integral method. This requires that the tradeoffs of loss attenuation and output accuracy be accounted for in the complete transfer function of the system.

Given the fact that the magnitudes of both methods are bounded and that the resulting signal will need to be fed into a saturation block and another SOGI filter, the derivative method
has been chosen to be implemented in this work because it is not sensitive to initial conditions and requires no additional losses or subsequent loss compensation.

Figure 6.8 illustrates the block diagram of the feedback compensation voltage control which includes a saturation block, a post-filter, and harmonic notch filters. The saturation block is used to limit the compensation voltage in order to limit the voltage response of the Hybrid Method given scenarios where there is low shunt impedance and high fault current from the device under test. In the practical implementation, the saturation level is parameterized on a per phase bases in order to allow for flexibility in adapting the feedback compensation voltage drop to the fault characteristics of the device under test for a given fault scenario.

![Block diagram of the voltage saturation block, the post-filter, and the harmonic cancelation filters.](image)

Figure 6.8: The block diagram of the voltage saturation block, the post-filter, and the harmonic cancelation filters.

However, the introduction of a non-linear control element with respect to saturation results in harmonic content added to the resulting output waveform if the saturation limits are reached. In order to overcome this problem and better constrain the ultimate output of the control to the fundamental frequency, a post-filter coupled with harmonic notch filters are employed. All of these filters are based upon the SOGI filter structure. There are four harmonic
notch filters designed to offer high attenuation of the complete control to the 2nd through 5th harmonic. Equation 6.2 demonstrates the equivalent transfer function of the post-filter and harmonic notch filters.

\[ H(s) = H_{post}(s) \left( 1 - \sum H_N(s) \right) : N = 2, 3, 4, 5 \quad 6.2 \]

Due to the high degree of attenuation desired, the SOGI filter gain of the harmonic notch filters is set much lower than the nominal SOGI filter gain and is equal to 0.05. This low gain results in a very narrow pass band on the harmonic SOGI filters. Given that they are subtracted from the unity gain feed-through from the post-filter, the harmonic SOGI filters appear as very narrow stop bands. Even though the SOGI filter gain utilized for the harmonic filters is very narrow, there still exist some fundamental frequency components that will impact the overall phase shift of the resulting waveform. Nevertheless, this can be counteracted by adjusting the pass band frequency of the post-filter with minimal impact to the overall filter gain. The revised frequency of the post-filter can be calculated by equating the resulting phase of equation 6.2 to zero. For a 60 Hz fundamental, the frequency of the post-filter that results in zero overall phase shift is roughly 63.3 Hz with an overall filter gain of 0.9983 instead of unity.

To demonstrate the functionality of this part of the feedback compensation voltage control, Figure 6.9 illustrates an input waveform to the saturation block and the resulting output after the post-filter and harmonic filters given heavy saturation. The saturation limit is set to one half and the input waveform’s amplitude is subjected to a rectangular step from 0.5 to 2.
Before looking at the response of the complete feedback compensation voltage control, an aspect to the practical implementation of the post-filter and harmonic filters must be noted. Given the transfer function in equation 6.2, it could be assumed that calculation of the post-filter and harmonic filters as a single transfer function could be an attractive method. However, this is not the case for two distinct reasons. First, if the individual SOGI transfer functions are all solved independently, the exact same subroutine can be used for all of the SOGI filters in the complete control system. The second, and more important, issue is that when the transfer function is combined as in equation 6.2, the zeros of the resulting transfer function move to mirror the pole locations of the harmonic filters along the imaginary axis.

Figure 6.10 illustrates the pole-zero map of the equivalent transfer function as shown in equation 6.2. Figure 6.11 shows the pole-zero map of the individual transfer functions with all of their zeros at the origin. This typically does not pose a problem when solving these transfer functions in a floating point arithmetic environment, such as MATLAB. However, when moved
to a fixed point arithmetic environment of a digital signal processor or an FPGA, the resulting transfer function will become unstable without excessively long factional bits. Thus, the transfer functions should be solved within the controller as individual transfer functions and efforts to combine transfer functions should be closely evaluated.

Figure 6.10: The pole zero map of the combined transfer function of the post-filter and four harmonic filters tuned to the 2$^{\text{nd}}$, 3$^{\text{rd}}$, 4$^{\text{th}}$ and 5$^{\text{th}}$ harmonics.

Figure 6.11: The pole zero map of the individual transfer functions of the post-filter and 4 harmonic filters tuned to the 2$^{\text{nd}}$, 3$^{\text{rd}}$, 4$^{\text{th}}$ and 5$^{\text{th}}$ harmonics.
Having evaluated the two halves of the feedback compensation voltage control, the response of the entire system can be evaluated. Figure 6.12 demonstrates the Bode plots of two feed-through paths, the direct path (resistive voltage drop calculation) and the quadrature, discrete difference path (inductive voltage drop calculation). As was stated earlier, the frequency response of these two paths is inherently different, but good attenuation of high order harmonics is provided by the harmonic notch filters and the resulting attenuation after the 5th harmonic is -10 dB.

![Bode Plots of the Direct and Difference Feedthrough Paths](image)

Figure 6.12: The Bode plots of the direct feed-through, resistive voltage calculation path and the difference feed-through, reactive voltage calculation path.

Figure 6.13 demonstrates the linear time domain response of the quadrature output voltage and the normalized integral of the quadrature output voltage to an example input current that contains characteristics of a fault current scenario. The example input current has a rectangular step in magnitude from 0.5 to 2 with a DC offset of 1 and is followed by the addition of the fundamental component with a second harmonic of 0.75 in magnitude. The saturation limits in this waveform are set to 0.5.
Figure 6.13: The linear time domain response of the quadrature feed-through path given an example input waveform consisting of a rectangular step in magnitude with a DC offset followed by a second harmonic addition to the fundamental. The output voltage and the normalized integral of the output voltage are shown.

As demonstrated in Figure 6.13, the design objectives of the feedback compensation voltage control are generally achieved with acceptable performance. Saturation was introduced into the control loop. The resulting waveform is nearly constrained to the fundamental component and the integral of the normalized output voltage is bounded and symmetrical about the axis. It can be stated that the gains and frequencies chosen within this dissertation might not be optimal with respect to the complete control algorithm; future work into this research area will likely result in better performance by improving upon the foundation presented here.
Feedback Compensation Voltage Bypass Switch and Transition Control

The logic and timing associated with the series bypass switches and the transitions in the complex vector calculation of the series impedance voltage drop operate on a completely phase independent basis. The reasoning behind this is that the insertion and removal of the series impedance requires precise control over both the switch states and the transition of the compensation voltage. In order to promote transitions in the series impedance without transients, the series bypass switch should be opened and closed when there is zero current flowing in the series impedance. This implies that the instantaneous energy stored in the reactive elements is balanced between both sides of the series impedance. The insertion of the series impedance on all three phases is not required of the overall Hybrid Method but will be assumed within this dissertation. Figure 6.14 illustrates the signal logic and timing associated with the feedback voltage compensation control. All of the variables associated with the logic are parameterized in the control algorithm.

Series Bypass Switch Timing Logic

![Diagram showing series bypass switch timing logic]

Figure 6.14: The single phase representation of the timing and logic for the series bypass switches. The rectangular traces indicate digital logic of the signals and the switch states.
In Figure 6.14, there are two distinct waveforms, the measured device under test output current waveform and a saw tooth waveform that represents an angular calculation obtained from the current measurement. The zero cross detection and angular calculation is performed after the pre-filter to ensure higher resiliency to multiple zero crossings. Additionally, there are three states used within the control logic: Arm Switch, Switch Impedance, and Switch State. The arm switch state is used to change the state of the series bypass switches by the master state machine controller and is the only input to the three series switch logic controls. Typically, the Arm Switch state transitions at the exact same time for all phases but the resulting timing and logic are independent on each phase.

On a per phase basis, once the Arm Switch state has transitioned high, the logic waits for the appropriate angle, Angle On, to transition the impedance values used in calculating the compensation voltage and turning on the switch pulse. It should be noted that, with the series bypass switch logic, the Switch Pulse state and Switch Action state shown in Figure 6.14 are inverted in order to control or represent the actual physical switch. Once the physical series bypass switch has received the command to open, it will not actually do so until the next zero crossing of the current. In the logic depicted, the transition in the compensating voltage is begun before the switch actually opens and is desired as the impedance transition must flow through the SOGI based post-filter.

When the Arm Switch state goes low, the logic waits for the appropriate angle, Angle Off, in which to transition the impedance values back to the bypassed state in the feedback compensation voltage control. However, the Switch Pulse and inherent Switch Action are delayed until the next zero crossing is detected, thus the series bypass switch is closed near a zero crossing.
To verify and validate the design and control of the Hybrid Method, a Controller Hardware-In-the-Loop (CHIL) experiment has been set up. In CHIL experiments, the actual control algorithms and control system hardware are interfaced against a real-time simulation of the physical system. The method of using CHIL experiments to validate both the control system algorithms and hardware is an increasingly more common practice as reported in the literature [49], [50], [51] and has been made possible by improved modeling and computing capabilities.

The rising importance of CHIL validation can be directly contributed to increasingly more complex controller designs and physical systems being implemented in almost all areas of engineering. This is especially true when the physical system is cost prohibitive to reproduce or maintain. One area of CHIL testing that has gained significant traction is the end of line testing of Engine Control Units (ECUs) of modern vehicles [52]. In such an application, the initial costs and continuous maintenance costs of replicating the actual physical system can be eliminated by simply modeling the physical system in real-time.

With respect to applications involving power systems and power electronics, the adoption of CHIL as a method of controller validation and verification has been widely accepted, especially in the area of protective relays [53], [54]. In fact, the Real Time Digital Simulator (RTDS) utilized in this work to simulate the physical system of the Hybrid Method was initially started as a research project at the Manitoba HVDC Research Centre and focused on the specific application of verifying a controller designed for the control of synchronous compensators at an HVDC terminal [55]. The RTDS system is a fully digital real-time power system simulator that is fundamentally based on Dommel’s solution approach for electromagnetic transients [56].
The application of the RTDS with respect to CHIL applications had been heavily used in the design, verification, and validation of electronic power system protective relays and advanced relay protection schemes. In the CHIL testing of protective relays, the physical system of a large, interconnected, power system is simulated in real-time on the RTDS. The measurements from various points within the simulated system are replicated to the physical protective relays, where the protective relays respond as if they were physically installed on the simulated system.

The CHIL experiments presented in this work are intended as an initial proof of concept of both the physical system and the vector controller of the Hybrid Method. The physical system of the Hybrid Method is to be simulated on a Real Time Digital Simulator (RTDS) and the vector controller of the Hybrid Method is implemented in the onboard Field Programmable Gate Array (FPGA) of a National Instruments Multifunction RIO 7842R. Figure 7.1 illustrates the complete block diagram of all of the components utilized in the controller hardware-in-the-loop experiments.

In Figure 7.1, there exist four main components to the Hybrid Method CHIL experiments: the Hybrid Method Controller, the Hybrid Method Physical System, the Hybrid Method Development Human Machine Interface (HMI), and the RTDS Runtime Engine. The remainder of this chapter will discuss the details of modeling the physical system on the RTDS and the implementation of the Hybrid Method vector control algorithm on the FPGA.
The Hybrid Method Controller contains both a high speed digital signal processing (DSP) loop and the Hybrid Method state machine. Both are implemented on the Xilinx Virtex 5 LX50 FPGA of the Multifunction RIO PXi 7842R card. The Hybrid Method Development HMI is implemented on the controller of the PXi chassis in which the Multifunction RIO is installed and direct communication between these two is made possible through the inner workings of the NI LabVIEW FPGA Module.

The Hybrid Method Physical System is simulated on a Real Time Digital Simulator (RTDS) consisting of two racks with four PB5 processors per rack. The RTDS Runtime Engine
is implemented on a standalone workstation and is interfaced to the RTDS through local Ethernet and the RTDS software suite.

**RTDS and Controller Communication Interfaces**

Figure 7.1 also demonstrates the communication paths between the RTDS simulation of the physical system and the National Instruments implementation of the vector controller. The communications between these two systems are broken into two distinct paths. The first communications path contains analog and digital communications between the FPGA and the RTDS. These analog and digital communications are locally wired between the inputs and outputs of each system and represent the instantaneous data shared between the two systems. This data includes the measured current at the point of common coupling as simulated in the RTDS, the digital solid-state AC switch states commanded by the controller and the voltage references generated by the vector controller.

The second communications path consists of a MODBUS TCP/IP communications link between the RTDS Runtime Engine workstation and the Hybrid Method Development HMI PXI chassis. The MODBUS communication is utilized to dramatically reduce the local digital IO required for configuration of the complete Reactive Divider Network between both environments. The configuration of this communication link is somewhat awkward because the RTDS Runtime Engine scripting tool is only capable of operating as a MODBUS master and the Hybrid Method Development HMI must act as the slave. It would be preferable for the HMI to push values to the RTDS Runtime Engine but this is overcome by setting up the RTDS Runtime Engine to poll the MODBUS registers of the slave HMI controller. There is also some
handshaking that is done to initialize and monitor this communication link on both ends that is not included in this discussion.

*High Level Controller Hardware-In-the-Loop Implementation*

The programmatic flowchart, shown in Figure 7.2, illustrates the high level interaction between the Hybrid Method Development HMI and the RTDS Runtime Engine. The logic outlined in the flowchart involves the configuration of the Reactive Divider Network between the physical system model, where tap switch states must be set, and the vector controller, where the impedances must be calculated. The details of the two sub processes, the FPGA Controller, and the RTDS Simulation Model will be outlined in the next sections of this chapter.
Hybrid Method Vector Controller Implementation

As previously mentioned, the Hybrid Method vector controller is implemented on a National Instruments PXI chassis with an R-Series 7842R Multifunction RIO card with an onboard Virtex 5 LX50 FPGA. This platform provides excellent flexibility with respect to implementing the real-time vector controller because the controller can be separated into two parts – one part that requires high speed digital signal processing and the other part that handles...
the entire human machine interface. Thus, the high priority, time critical tasks can be performed on the FPGA and communication between the host controller running the HMI and the FPGA can be performed seamlessly within the LabVIEW development environment. In this section, only a brief overview of the controller will be presented and the LabVIEW virtual instruments are documented in Appendix A.

**FPGA Real-Time Controller Processing Loops**

This section discusses the implementation of the Hybrid Method vector controller within the FPGA. One of the main benefits of implementing the vector controller in an FPGA comes from the fact that FPGAs are inherently capable of parallel processing and have very deterministic timing characteristics. In fact, FPGAs tend to blur the lines drawn between hardware and software, as they allow for a high degree of customization through reprogramming but have the timing and reliability of hardware. With the inclusion of dedicated Digital Signal Processing (DSP) slices on newer FPGA models, the applications for FPGA has begun to overlap more with the conventional embedded computing RISC and DSP architectures.

The FPGA utilized in this application is a Xilinx Virtex 5 LX50, and when coupled to the NI PXIe 7842R card, offers 96 digital IOs, 8 analog inputs, and 8 analog outputs, all accessible from the FPGA. This is ideal for the Hybrid Method CHIL experiment because the FPGA can be interfaced directly with the RTDS IO cards. With respect to the FPGA size, Table 7.1 indicates the fabric utilization on the LX50. It is clear that if significant additional logic were needed to be implemented on the FPGA, a larger size FPGA would be required. However, with respect to the timing performance of the FPGA, the control loops illustrated below are capable of running at over 30 kHz. The loop clock of the FPGA is intentionally slowed down to 10 kHz for
better emulation of the reference sampling bandwidth of the SCHB power converter, which is 12 kHz, while maintaining a multiple of the RTDS simulation large time step, which is 20 kHz.

Table 7.1: Virtex 5 LX50 Device Utilization Map

<table>
<thead>
<tr>
<th></th>
<th>Used</th>
<th>Total</th>
<th>Percent Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Slices</td>
<td>7196</td>
<td>7200</td>
<td>99.9</td>
</tr>
<tr>
<td>Slice Registers</td>
<td>25738</td>
<td>28800</td>
<td>89.4</td>
</tr>
<tr>
<td>Slice LUTs</td>
<td>24734</td>
<td>28800</td>
<td>85.9</td>
</tr>
<tr>
<td>DSP48s</td>
<td>34</td>
<td>48</td>
<td>70.8</td>
</tr>
<tr>
<td>Block RAMs</td>
<td>16</td>
<td>48</td>
<td>33.3</td>
</tr>
</tbody>
</table>

Figure 7.3 demonstrates the fundamental flowchart of the logic implemented within the FPGA. There are three separate loops running on the FPGA at one time. The first loop is the simple state machine implementation utilized to enforce the timing between the operational states of the Hybrid Method. This includes the time between inserting the series impedance and the start of the fault event, the length of the fault event, and the time after the fault invention before the series impedance is removed from the circuit. The other two loops make up the complete digital signal processing required for implementation of the vector controller.

The main digital signal processing loop on the FPGA computes the feed-forward reference control and feedback compensation voltage control, along with their complementary switching logic. As demonstrated in the previous chapter, both of the control loops feature Second Order Generalized Integrators (SOGI) within their control structure. Thus, to conserve fabric on the FPGA, a separate control loop was designed to solve the SOGI transfer functions. In total, there are 21 SOGI transfer functions, 7 per phase, that need to be calculated for each iteration of the complete control loop. Figure 7.4 demonstrates the basic block diagram for calculating a second order discrete time transfer function.
Figure 7.3: A flowchart of the FPGA loops, including the Hybrid Method state machine, the high speed digital signal processing loop, and the second order generalized integrator sub-processing loop.

Figure 7.4: The block diagram of the direct form calculation of the SOGI fixed point discrete transfer function.
Each of the 21 transfer functions has a reserved memory space that contains the transfer function coefficients, the previous output and input, as well as the intermediate states of each SOGI filter represented in Figure 7.4 as zero-order hold functions. In order for the SOGI sub-process loop to calculate the output for all 21 transfer functions independently, the latest input value is set in memory for the specific SOGI transfer function by the main DSP loop. The requests to the SOGI sub-process loop is made by pushing the transfer function memory address, 1 through 21, onto a FIFO buffer. Within the SOGI sub-process loop, the FIFO buffer is continuously polled and if an element is present, the memory address for the transfer function is pulled off of the FIFO. The sub-process loop then performs the transfer function calculation based upon what is read from memory, writes the new intermediate states and the new output back to memory, and pushes the memory address onto another FIFO that is acknowledged in main DSP loop.

The feed-forward reference voltage control and the feedback compensation voltage control operate in parallel with the logic and timing associated with each control loop as depicted in the previous chapter. Figure 7.5 illustrates the logic implemented on FPGA for the shunt fault switch in order to achieve the order of operations that was depicted in Figure 6.3. Figure 7.6 illustrates the logic implemented on FPGA for the series bypass switch in order to achieve the order of operations that was depicted in Figure 6.14.
Figure 7.5: The logic implementation for the shunt switch action

Figure 7.6: The logic implementation for the series bypass switch action
Since the vector control algorithms have been implemented on an FPGA, the calculations performed must be completed in fixed point arithmetic instead of floating point arithmetic common to personal computers. Additionally, the values read from the analog input and written to the analog output channels are of a 16 bit signed integer format that correspond to a +/-10 V analog range. Thus, to achieve the maximum fidelity when working with a fixed point number system, the scaling of these values and that of the constants used in calculations becomes very important. There are several automated scaling programs designed to discretize and convert transfer functions of the SOGIs to ensure proper conversion. These have been utilized within this work for the SOGI transfer functions.

However, there is a fair bit of scaling required with respect to the feedback voltage compensation control for calculating the base impedance and the intended maximum range of the ultimate reference voltage which is transmitted as a modulation index to the SCHB power amplifier. To maximize the quantization of the analog signals and utilize the full range of the inherent 16 bit integer to 10 V analog signal ratio, the modulation signal to the SCHB power amplifier is used as the voltage base within the controller. Since the range of modulation signal is constrained to being on the interval of -1 to 1, a direct calculation can be obtained to determine the nominal modulation given the regulated DC bus voltage, 1100 V, and the desired output voltage, 4160 V. Equation 7.1 demonstrates the calculation of the voltage base of the vector controller based upon a 16 bit signed integer, where the most significant bit represents the sign of the number.

$$V_{\text{Base}-16} = \frac{2^{15}}{4\sqrt{3} V_{DC} / \sqrt{2} (4160 \text{ V})} = 25296$$  \hspace{1cm} 7.1
The result in equation 7.1 is equivalent to a modulation index of roughly 0.772 and represents the nominal voltage of 4160 V from the terminals of the SCHB power amplifier. Further, it is equivalent to the base voltage of 23.9 kV at the point of common coupling after the step-up transformers assuming an ideal voltage ratio.

Likewise, the scaling of the current feedback from the RTDS simulation can be scaled such that a maximum expected current is represented by a 10 V analog signal coming from the RTDS analog output. In this dissertation, the maximum expected current is set to be 2500 A peak, which approximately corresponds to a fault duty of 100 MVA on the physical system. The vector controller base current on a 16 bit signed integer scale can then be calculated given the nominal peak base current of the physical system. Equation 7.2 demonstrates the calculation of the vector controller base current given a power base of 15 MVA and a voltage base of 23.9 kV at the point of common coupling on the physical system.

\[ I_{\text{Base-116}} = \left( \frac{\sqrt{2} (15 \text{ MVA})}{\sqrt{3} (23.9 \text{ kV})} \right)^{2^{15}} = \frac{2500 \text{ A}}{2500 \text{ A}} = 6718 \]

Since the feedback compensation voltage control of the vector controller requires the conversion of current into voltage by Ohm’s law, the two calculated vector controller base current and voltage can be utilized to determine the per-unit base impedance.

\[ Z_{\text{Base-FP}} = \frac{V_{16\text{Base}}}{I_{16\text{Base}}} = 3.76541 \]

Utilizing the result in equation 7.3, the per unit impedances of the reactive divider network as measured on a 15 MVA base at 23.9 kV can be easily converted to the vector controller base quantities by multiplying them by the resulting vector controller base impedance.
This process is done in the Hybrid Method Development HMI controller to best utilize the FPGA resources. The result is converted to a fixed point representation of the series impedances before being transmitted down to the FPGA. The series impedances within the vector controller are represented with a 16 bit fractional portion that results in an impedance resolution of approximately 1.5 thousandths of a percent impedance. Thus, a very accurate representation of the series impedance is achieved within the vector controller and limited quantization error is obtained within the complete controller.

Real-Time Digital Simulation of the Hybrid Method Physical System

A Real Time Digital Simulator (RTDS) is used to model the Hybrid Method’s physical system such that the physical system can be simulated in real-time in order to verify the real-time operation of the Hybrid Method vector controller. For the purposes of this research, only a brief introduction into the modeling capabilities of the RTDS environment will be discussed with a more thorough explanation to be found within the RTDS manuals [56].

The characteristic of the RTDS system utilized in this research consists of two RTDS racks that contain four PB5 processors per rack. The RTDS racks communicate with the workstation PC using the RTDS Runtime software through TCP/IP over Ethernet.

Within the RTDS, there are two possible simulation modes, one consisting of large time step simulations with typical time steps of 50 μs and another consisting of small time step simulations with typical time steps from 2 to 3 μs. The large time step simulations are most applicable to large power system models and are able to realistically resolve transient simulations into the 2 to 3 kHz ranges. However, whenever power electronics are utilized within
a system model, the small time step simulations offer greater resolution of the switching transitions involved. The large and small time step simulations can be connected through special interface transformer models that resolve the inherent time step issues.

The communication between processors for large time step simulations is provided through the physical backplane of the RTDS rack with the resulting time delay resolved through the use of transmission lines in the simulation model. With respect to small time step simulations, the RTDS backplane does not offer the latency required to ensure only one time step of transmission delay. Hence, the processors solving the small time step simulations must be connected directly via fiber optic cables and the models must utilize small time step transmission line models to resolve the inherent transmission delay between processors. Additionally, the number of switching devices capable of being resolved within a small time step is limited to 32 individual switches, which limits the amount of detail that can be simulated in a single small time step simulation. It is possible to span a small time step simulation between both of the processors on a PB5 card. However, this does not resolve the 32 switch limit but does allow for the simulation time step to be reduced given added complexities of the small time step model.

For the research presented here, the entire physical system of the Hybrid Method is parsed amongst the PB5 processor cards in small time step simulations such that the complete physical system, including the devices under test, are modeled in the small time step. However, the small time step is generally only suitable for resolving the electromagnetic transient problem including the power electronic switch states and does not typically contain any of the controls for these power electronic devices other than carrier wave signals instrumental to precise switch timing. Instead, the controls for the analog and digital IO, the SCHB power amplifier active front ends, and the device under test are simulated in what is referred to as control processors.
within the RTDS. These control processors have time steps and communication speeds consistent with the large time step simulations and are able to communicate with the small time step simulations through the RTDS backplane.

Figure 7.7 illustrates the mapping of the Hybrid Method physical system with the device under test into small time step simulation blocks on RTDS PB5 processor cards as well as the control processors utilized for the simulation of various control elements. With respect to the hybrid physical system, the physical system is broken down on a phase basis into three PB5 processor cards. The SCHB power amplifier and the step-up transformer are modeled on the first processor of the PB5 card and the reactive divider network is modeled on the second processor of each card. These two small time steps are connected via a small time step transmission line with the minimum transmission line parameters required by the time step to result in a very stiff connection in the model. The point of common coupling of the reactive divider networks for all three phases are then combined through small time step transmission lines to the PB5 processor card on the second rack that is simulating the device under test. Additionally, not shown in Figure 7.7 for clarity purposes, the neutral bonding point of each of the reactive divider networks on phase A and phase C are connected to create a common neutral bonding point on phase B.
The mapping of the Hybrid Method physical system with the device under test onto small time step simulations running on the PB5 processor cards spanning across two RTDS racks.

The complete, interconnected small time step simulation shown in Figure 7.7 is able to be simulated at a time step of 3.333 μs. This is just slightly outside the recommended range of 2 to 3 μs for maintaining the accuracy with respect to the switching losses of the devices. The slightly larger time step is driven by the processing burden placed upon the phase B reactive divider network small time step simulation by the resolution of several small time step transmission lines. Future work will consider, in more detail, the modeling parameters of the individual devices in order to achieve an optimal solution. This may involve moving the reactive
divider network simulations into a single large time step simulation for reasons that will be discussed later in this chapter.

*Medium Voltage, Multi-Level Power Amplifier RSCAD Model*

With respect to the modeling of the medium voltage, multi-level Series Connected H-Bridge (SCHB) power amplifier, the focus is placed on the output stage of the amplifier. A suitable equivalent system for the active front end and DC bus characteristics is utilized to model the SCHB power amplifier in real-time on the RTDS system as described earlier. As discussed in Chapter Four, when describing the physical system, the SCHB power amplifier model is a parallel equivalent of the eight individual SCHB power amplifier sections.

Thus, the equivalent model of the power amplifier output stage has the base output ratings of 15 MVA at 4160 V. The individual valve parameters for each of the equivalent H-bridges are given in Table 7.2. The switching frequency is held at 600 Hz for this dissertation and results in the first noise mode being centered on 4800 Hz. This provides a good balance between the conduction and switching losses for an application that will require over-current capabilities.

<table>
<thead>
<tr>
<th>Table 7.2: RTDS Equivalent Power Amplifier Output H-Bridge Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Amplifier H-Bridge Parameters</strong></td>
</tr>
<tr>
<td>Valve Voltage</td>
</tr>
<tr>
<td>Valve Current</td>
</tr>
<tr>
<td>Valve Damping Factor</td>
</tr>
<tr>
<td>Valve Base Frequency</td>
</tr>
<tr>
<td>Valve Parallel Resistance</td>
</tr>
<tr>
<td>Carrier Wave Frequency</td>
</tr>
</tbody>
</table>
The model of the SCHB power amplifier’s active front end and DC bus’ dynamics are modeled as a linear system instead of a three phase PWM rectifier and DC bus capacitor in order to limit the number of small time step simulations required. The demarcation between the linear simulation of the power amplifier input stage and the non-linear PWM switched output stage is made at the DC bus capacitance because this point offers a high degree of attenuation of the underlying switching noise created by the active front end PWM rectifier.

The DC bus of each of the individual H-Bridges in the equivalent power amplifier output stage are modeled as voltage controlled sources. The voltage control for DC bus sources is taken from the approximate linear equivalent circuit of the active front end and dc bus dynamics. The voltage oriented control demonstrated in Figure 4.9 is coupled with the linear model of the isolation impedance and DC bus capacitance shown in Figure 7.8 to generate a scaled approximate equivalent DC bus dynamics. The current feedback is scaled by one eighth from the parallel equivalent output to represent one of the eight individual active front ends. Assuming the parallel equivalent output has perfect current sharing, the DC bus dynamics between all eight individual sections should be identical. Table 7.3 contains the parameters of the linear equivalent system and the voltage oriented control used to regulate the DC bus voltage.

![Figure 7.8](image_url)  
**Figure 7.8:** The linear physical system model of the active front ends including a linear isolation impedance and DC bus capacitance.
In order to further simplify the linear approximation made for the DC bus dynamics when coupled to the detailed output stage, the linear approximation of the DC bus voltage is replicated for each of the individual H-Bridges within a single phase. This is made possible by the fact that the voltage reference waveforms for each of the H-Bridges are only offset by 45° of the carrier waveforms, which operate well above the fundamental frequency. Thus, the voltage sources created by each of the H-Bridges are practically in phase with each other and the DC bus dynamics should be similar. Figure 7.9 demonstrates the DC bus voltage dynamics for all four H-Bridge output sections with independent linear approximate active front end models. It can be seen that all of the DC bus voltage dynamics follow the same trajectories in the upper plot. 

<table>
<thead>
<tr>
<th>Linear Physical System Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation Impedance Resistance</td>
</tr>
<tr>
<td>Isolation Impedance Inductance</td>
</tr>
<tr>
<td>DC Bus Capacitance</td>
</tr>
<tr>
<td>RL Circuit Gain (1/R)</td>
</tr>
<tr>
<td>RL Circuit Time Constant (L/R)</td>
</tr>
<tr>
<td>DQ Decoupling Term (ω*L)</td>
</tr>
<tr>
<td>Capacitor Gain (2/C)</td>
</tr>
<tr>
<td>AC Phase Voltage (RMS)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DC Bus Voltage Regulator Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportional Gain</td>
</tr>
<tr>
<td>Integral Gain</td>
</tr>
<tr>
<td>Anti-Windup Gain</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DQ Current Regulator Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportional Gain</td>
</tr>
<tr>
<td>Integral Gain</td>
</tr>
<tr>
<td>Anti-Windup Gain</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DC Bus Voltage Feedback Notch Filter (SOGI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Filter Gain (k)</td>
</tr>
<tr>
<td>Filter Frequency (ω)</td>
</tr>
</tbody>
</table>

Table 7.3: RTDS Power Amplifier Active Front End Linear Approximation and Control Parameters
is demonstrated by the minimal error between the first DC bus voltage and the other three DC bus voltages. Thus, only one linear approximate active front end model is needed per phase to account for the DC bus dynamics in the complete simulation of the SCHB power amplifier.

Figure 7.9: A comparison of 4 independent AFE’s DC bus voltage values during a 1 pu resistive step change in load from 0.06 seconds to 0.16 seconds.

**Step-Up Transformer RSCAD Model**

Just like the SCHB power amplifier, the step-up transformer between the power amplifier and the reactive divider network is a parallel equivalent of the two single phase transformers. Since the transformer design of utilized in the Hybrid Method physical system is a single-phase design, it lends itself very well to modeling in the small time step as discussed earlier. The parallel equivalent single phase transformer model is rated at 5 MVA instead of 2.5 MVA. Table 7.4 contains the parameters of the parallel equivalent single phase transformer model.
Table 7.4: RTDS Power Amplifier Step-Up Transformer and Saturation Characteristic Parameters

<table>
<thead>
<tr>
<th>Winding Configuration</th>
<th>Single Phase Yy</th>
</tr>
</thead>
<tbody>
<tr>
<td>LV Winding Voltage</td>
<td>2.4 kV</td>
</tr>
<tr>
<td>HV Winding Voltage</td>
<td>13.8 kV</td>
</tr>
<tr>
<td>Rated Power</td>
<td>5 MVA</td>
</tr>
<tr>
<td>Rated Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>HV Winding Reactance</td>
<td>0.035 pu</td>
</tr>
<tr>
<td>LV Winding Reactance</td>
<td>0.015 pu</td>
</tr>
</tbody>
</table>

Saturation Characteristics Parameters

<table>
<thead>
<tr>
<th>Slow Flux Time Constant</th>
<th>5 sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Power</td>
<td>5 MVA</td>
</tr>
<tr>
<td>Rated Voltage</td>
<td>2.4 kV</td>
</tr>
<tr>
<td>Rated Frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Magnetizing Current (% Irated)</td>
<td>0.50%</td>
</tr>
<tr>
<td>Air Core Inductance</td>
<td>0.045 pu</td>
</tr>
<tr>
<td>Flux Knee Point</td>
<td>1.45 pu</td>
</tr>
<tr>
<td>Hysteresis Loop Width (%)</td>
<td>10%</td>
</tr>
</tbody>
</table>

The magnetic saturation of the transformer core is modeled with a small time step saturation block and adheres to the magnetic flux versus magnetizing current curve defined by equation 7.4. Unlike most transformer saturation models where the saturation block is placed outside of the equivalent leakage reactance, the transformer saturation is modeled on the low voltage winding of the transformer and is located between an equivalent low voltage leakage reactance and high voltage leakage reactance. By placing the saturation between two equivalent leakage reactances, the effect of large step changes in load current will result in a shift in the flux operating point due to the voltage drop induced across the low voltage leakage reactance. This would not happen if the saturation block was placed directly at the terminals of the SCHB power amplifier and is viewed as a better representation of the true physical system.
\[ I_S = \left[ \sqrt{(\Phi_S - \Phi_K)^2 + 4DL_A + (\Phi_S - \Phi_K)} \right] \frac{D}{\Phi_K} \]

\[ A = \frac{L_A}{\phi_K^2} \quad B = \frac{L_A I_M - \phi_M}{\phi_K} \]

\[ C = I_M (I_M L_A - \phi_M + \phi_K) \quad \phi_M = \frac{V_M}{2\pi f} \]

\[ D = \frac{-B - \sqrt{B^2 - 4AC}}{2A} \]

\[ \phi_K = K \phi_M \]

Taking into account the continuous overvoltage capabilities and the 50 Hz rating of the transformer, Figure 7.10 demonstrates the saturation curve of the transformer as modeled, with labels for the 50 and 60 Hz operating conditions. Additionally, as is typical with the saturation model demonstrated in equation 7.4, hysteresis is simulated by shifting the magnetizing curve along the magnetizing current axis in both directions by some percentage of the rated magnetizing current. Figure 7.11 demonstrates the hysteresis loop modeled for the step-up transformer in the RTDS.

Figure 7.10: The transformer core saturation characteristics of the parallel equivalent single phase transformer model.
Figure 7.11: The hysteresis loop of the parallel equivalent single phase transformer model.

Reactive Divider Network RSCAD Model

Much like the SCHB power amplifier and the step-up transformer, the reactive divider network is modeled on a single phase basis. This is necessitated by the number of switches that are contained within the per phase reactive divider network. The model of the reactive divider network implemented in RSCAD is very similar to that presented in Figure 4.12. However, the main difference is that the six position tap selector switches for the variable resistances and inductances are replaced with five discrete on/off switches connected in a bypass configuration as demonstrated in Figure 7.12. Table 7.5 contains the parameters of tapped resistors and inductors, the fixed inductor parameters and the switch characteristics for both the equivalent tap switch bypass switches and the LDRT switches utilized to switch in and out the fix inductors. The inductors are assumed to have a quality factor of 40 at 60 Hz and the resistors are assumed to be ideal.
Figure 7.12: The model equivalent of a 6 position tap switch through the use of five equal discrete impedances and five discrete bypass switches.

Table 7.5: RTDS Reactive Divider Network and Tap Switch Parameters

<table>
<thead>
<tr>
<th>Physical Impedance Element Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tapped Resistor Resistance Per Step</td>
</tr>
<tr>
<td>Tapped Inductor Inductance Per Step</td>
</tr>
<tr>
<td>Tapped Inductor Resistance Per Step</td>
</tr>
<tr>
<td>Fixed Inductor Inductance</td>
</tr>
<tr>
<td>Fixed Inductor Resistance</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tap and Fixed Switching Devices Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valve Voltage</td>
</tr>
<tr>
<td>Valve Current</td>
</tr>
<tr>
<td>Valve Damping Factor</td>
</tr>
<tr>
<td>Valve Base Frequency</td>
</tr>
<tr>
<td>Valve Parallel Resistance</td>
</tr>
</tbody>
</table>

One issue with the way in which the reactive divider network has been modeled involves the method in which RTDS models the valve parameters within the small time step simulation. As the switches in the physical system utilize an actual air gap with respect to the six position tap switches or a contact gap in vacuum with respect to the LDRT switches, the switches implemented in the reactive divider network physical system will exhibit little to no leakage current under all nominal operating conditions. However, because the valves are modeled in the small time step as an inductance when the switch is on and a series resistive capacitive circuit when the switch is off, there exists a significant amount of parasitic impedances within the model that are not indicative of the actual physical system. This method of modeling is used in the small time step simulations because it does not require inversion of the conductance matrix so
long as the Dommel conductance of the series RC circuit is equivalent to that of the inductance in the switch model [56].

Future work will resolve these modeling issues by adjusting the valve parameters in the small time step but the ultimate solution might be to convert the reactive divider network models to the large time step where the conductance matrix is inverted for each time step. Nevertheless, the issues associated with this problem are well outside of the frequency band of the Hybrid Method vector controller and do not significantly impact the results within this research.

Also included in the model of the reactive divider network are the equivalent solid-state AC switches. While the physical switch is comprised of several thyristors stacked in series with their own independent RC snubber circuits as demonstrated in Figure 4.14, the equivalent solid-state AC switch model contains a single back to back valve model with an equivalent RC snubber circuit in parallel. Table 7.6 contains the parameters for the equivalent solid-state AC switch and the equivalent snubber parameters. The equivalent snubber parameters are taken as the series combination of the individual snubber circuits, assuming the individual snubber circuits have a resistance of 40 ohms and a capacitance of 0.5 µF.

Table 7.6: RTDS Thyristor Equivalent Switch and Snubber Parameters

<table>
<thead>
<tr>
<th>Thyristor Equivalent Switching Devices Parameters</th>
<th>Thyristor Equivalent Snubber Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valve Voltage</td>
<td>Equivalent Snubber Resistance</td>
</tr>
<tr>
<td>35 kV</td>
<td>400 Ω</td>
</tr>
<tr>
<td>Valve Current</td>
<td>Equivalent Capacitance</td>
</tr>
<tr>
<td>0.5 kA</td>
<td>0.05 µF</td>
</tr>
<tr>
<td>Valve Damping Factor</td>
<td></td>
</tr>
<tr>
<td>0.9 pu</td>
<td></td>
</tr>
<tr>
<td>Valve Base Frequency</td>
<td></td>
</tr>
<tr>
<td>60 Hz</td>
<td></td>
</tr>
<tr>
<td>Valve Parallel Resistance</td>
<td></td>
</tr>
<tr>
<td>1 pu</td>
<td></td>
</tr>
</tbody>
</table>
Real-Time Digital Simulation of the Device Under Test

In order to demonstrate the performance of the Hybrid Method, two different devices under test models are utilized. The first model is a synchronous generator that is connected to the point of common coupling through a voltage matching transformer. This machine exhibits a large short circuit duty with asymmetrical components. The second device is a model of a doubly fed induction generator that is also connected to the point of common coupling through a voltage matching transformer. This machine exhibits a less severe fault duty but still maintains significant asymmetrical components. This section will discuss the model detail and parameters for both of these devices under test.

*Synchronous Generator RSCAD Model*

The synchronous generator model is intended to demonstrate the operation of the Hybrid Method under the more extreme fault scenarios that include both sub-transient and asymmetrical fault currents. This model is implemented using the small time step synchronous machine model found in RSCAD. It is coupled to the Hybrid Method physical system through a step-up transformer that has a delta primary connected to the point of common coupling and a wye secondary that is connected to the terminals of the synchronous generator as demonstrated in Figure 7.13.
The parameters for the synchronous generator and the step-up transformer are given in Table 7.7 and Table 7.8, respectively. The synchronous generator is rated for 10 MVA with a rated terminal voltage of 4160 V. The generator model is implemented without excitation control, governor control, or prime mover dynamics in order to demonstrate the fault characteristics of the machine alone. The modeled machine is driven with a constant torque of 1 pu with an excitation for unity power factor calculated at 1.45 pu field current. Modeling of the generator in this method will demonstrate the inherent stability of the Hybrid Method of fault ride-through evaluations because the machine has no external sources of damping or voltage regulation typically provided by power system stabilizer and voltage regulation excitation control. In fact, the machine is modeled with no frictional damping and the only transient damping of the swing equation is provided through the stator winding losses with the power being absorbed by the Hybrid Method physical system.
### Table 7.7: RTDS Synchronous Generator Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Generator Power</td>
<td>10 MVA</td>
</tr>
<tr>
<td>Rated Generator Voltage</td>
<td>4.16 kV</td>
</tr>
<tr>
<td>Rated Generator Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Inertial Constant (H)</td>
<td>1 MWs/MVA</td>
</tr>
<tr>
<td>Frictional Damping (D)</td>
<td>0 pu</td>
</tr>
<tr>
<td>Stator Leakage Reactance (Xa)</td>
<td>0.130 pu</td>
</tr>
<tr>
<td>D-axis Unsaturated Reactance (Xd)</td>
<td>1.1 pu</td>
</tr>
<tr>
<td>D-axis Unsat. Trans. Reactance (Xd')</td>
<td>0.36 pu</td>
</tr>
<tr>
<td>D-axis Unsat. Sub-Trans. Reactance (Xd&quot;)</td>
<td>0.2 pu</td>
</tr>
<tr>
<td>Q-axis Unsaturated Reactance (Xq)</td>
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</tr>
<tr>
<td>Q-axis Unsat. Sub-Trans. Reactance (Xq&quot;)</td>
<td>0.2 pu</td>
</tr>
<tr>
<td>Stator Resistance</td>
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</tr>
<tr>
<td>D-axis Unsat. Trans. Time Constant (Tdo')</td>
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</tr>
<tr>
<td>D-axis Unsat. Sub-Trans. Time Constant (Tdo&quot;)</td>
<td>0.075 sec</td>
</tr>
<tr>
<td>D-axis Unsat. Sub-Trans. Time Constant (Tqo&quot;)</td>
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</tr>
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<td>Zero Sequence Resistance</td>
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</tr>
<tr>
<td>Zero Sequence Reactance</td>
<td>0.01 pu</td>
</tr>
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</table>

### Table 7.8: RTDS Synchronous Generator Step-up Transformer and Saturation Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Winding Configuration</td>
<td>Single Phase – Dy</td>
</tr>
<tr>
<td>LV Winding Voltage</td>
<td>2.4 kV</td>
</tr>
<tr>
<td>HV Winding Voltage</td>
<td>23.9 kV</td>
</tr>
<tr>
<td>Rated Power</td>
<td>3.5 MVA</td>
</tr>
<tr>
<td>Rated Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>HV Winding Reactance</td>
<td>0.025 pu</td>
</tr>
<tr>
<td>LV Winding Reactance</td>
<td>0.0 pu</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow Flux Time Constant</td>
<td>5 sec</td>
</tr>
<tr>
<td>Rated Power</td>
<td>3.5 MVA</td>
</tr>
<tr>
<td>Rated Voltage</td>
<td>2.4 kV</td>
</tr>
<tr>
<td>Rated Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Magnetizing Current (% Irated)</td>
<td>1.00%</td>
</tr>
<tr>
<td>Air Core Inductance</td>
<td>0.05 pu</td>
</tr>
<tr>
<td>Flux Knee Point</td>
<td>1.2 pu</td>
</tr>
<tr>
<td>Hysteresis Loop Width (%)</td>
<td>10%</td>
</tr>
</tbody>
</table>
One aspect worth mentioning but somewhat outside of the scope of this research is the fact that the stability of the machine is defined by the swing equation of the synchronous machine. In the most basic form of the swing equation, an equal area criterion is utilized to determine the critical clearing angle of a fault such that the accelerating energy during the fault is balanced with the available decelerating energy after the fault in order to ensure that there will not be a pole slip of the generator. This can be somewhat exacerbated by modeling the system with a constant torque input because the acceleration of the generator during a fault is not limited by the torque and speed dynamics of a prime mover. However, this is not of the upmost importance with respect to this research so long as the fault duration is limited in time such that the machine will always remain stable. For the controller hardware-in-the-loop experiments presented here, the fault duration will be limited to 100 ms, not including the inherent clearing time of the shunt fault switches, in order to ensure that the fault is cleared prior to the critical clearing angle under all of the presented fault scenarios.

The step-up transformer is modeled as three separate single phase transformers that are connected in delta on the 23.9 kV primary and in wye on the 4160 V secondary. This is representative of a typical embodiment of small synchronous generator installations because of the resiliency to single line to ground faults on the primary, which are the most common type of fault on a power system. The transformer includes a phase shift between the primary and secondary. This will be illustrated in the results and show how the fault voltages are transformed through the transformer and the subsequent synchronous machine’s fault characteristics altered with what would be expected given only the voltages at the point of common coupling and the machine characteristics [57].
This will also reveal a challenge with the Hybrid Method as demonstrated in this work, where a single line to ground fault on this synchronous generator and transformer model will result in slightly higher than nominal current on a phase other than the one being faulted. However, this can be accommodated with more sophisticated configurations of the Hybrid Method than will be presented in this research and will be accounted for in future work. Nevertheless, this is not to say that the configuration methods and control of the Hybrid Method demonstrated in this work is not acceptable or would result in malfunction.

Saturation is modeled on the transformer and is applied directly to the wye secondary winding of the transformer. The saturation curve characteristic as modeled is not necessarily as conservative as what would be modeled for a large synchronous generator, 100’s of MW, for two reasons. Typically, in smaller applications, standard distribution transformer designs are utilized as a cost savings measure. This is especially true for wind turbine projects. Second, it is desired that the transformer exhibit magnetic saturation to demonstrate the decoupling of the magnetic flux between the Hybrid Method physical system and the device under test.

Doubly Fed Induction Generator RSCAD Model

Included in this research is a representative model of a Doubly Fed Induction Generator (DFIG) that is used to provide diversification to the device under test modeling and demonstrate the performance of the Hybrid Method with a more controlled fault characteristic. The DFIG model used in this research is modified from an example case that is shipped with RSCAD Version 3.03 and is representative of a generic 2 MW wind turbine DFIG. The model has been adapted to integrate with the model of the hybrid physical system by removing the large time step point of common coupling within the model and tying the step-up transformer directly to the
small time step transmission lines originating from the three reactive divider network small time step simulation blocks. The model has also been modified to include transformer magnetic saturation that is placed on the secondary winding connected directly to the DFIG stator.

This work will not discuss the details of modeling a DFIG as it is extensively covered in the literature and does not directly pertain to the demonstration of the Hybrid Method. Instead, the main components of the DFIG will be outlined and their operation briefly discussed in order to aid with interpretation of the results when evaluating the performance of the Hybrid Method. As demonstrated in Figure 7.14, the DFIG model contains four fundamental components: a three winding isolation transformer, a wound rotor induction machine, a back-to-back power electronic converter, and a high pass shunt filter. The parameters for the wound rotor induction machine and the three winding isolation transformer can be found in Table 7.9 and Table 7.10, respectively.

Figure 7.14: The schematic of the doubly fed induction generator modeled in RTDS.
Within the representative 2 MW DFIG model of a wind turbine generator, the blade set is mechanically coupled to the rotor of the induction machine through a multi mass gearbox model in order to increase the speed of rotation for the generator. The stator of the induction machine is connected directly to the isolation transformer. The back-to-back power electronic converter is utilized to maintain the power factor of the complete system while also providing the variable voltage, variable frequency rotor excitation to allow for a wide operating speed range. The variable voltage, variable frequency rotor excitation is calculated as the difference between the desired induction machine slip and the speed of the induction machine rotor as defined by the equations governing the induction machine.

The high pass shunt harmonic filter is utilized to attenuate the high order harmonic content associated with the PWM switching of the active front end of the back-to-back power electronic converter and also provide reactive power support at the fundamental frequency. The high pass shunt harmonic filter is tuned to the 40\textsuperscript{th} harmonic and delivers a fundamental reactive power of 200 kVAR. The back-to-back converter is also equipped with a crowbar circuit to dampen the fault current of the wound rotor induction machine that is reflected through the rotor during the initial part of a fault. The crowbar circuit is implemented as a controlled shunt resistance on the DC bus and is connected in parallel with the DC bus capacitance.

Depending on the manufacturer of the DFIG wind turbine generator, some alternative topologies can be employed with respect to the representative 2 MW model. It has become more common practice to utilize a two winding transformer with an isolation reactor between the transformer secondary and the active front end. The crowbar circuit is often implemented as a secondary circuit in parallel with the rotor side power electronic converter. The shunt harmonic filter is commonly a series RC type filter that is tuned with the series system inductances.
Table 7.9: RTDS Doubly Fed Induction Generator Parameters

<table>
<thead>
<tr>
<th>Doubly Fed Induction Generator Parameters</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Rated Generator Power</td>
<td>2.2 MVA</td>
</tr>
<tr>
<td>Rated Generator Voltage</td>
<td>0.69 kV</td>
</tr>
<tr>
<td>Rated Generator Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Inertial Constant (H)</td>
<td>1.5 MWs/MVA</td>
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<tr>
<td>Stator Resistance</td>
<td>0.0046 pu</td>
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<td>Stator Leakage Reactance</td>
<td>0.102 pu</td>
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<tr>
<td>Rotor Over Stator Turns Ratio</td>
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<tr>
<td>Unsaturated Magnetizing Reactance</td>
<td>4.35 pu</td>
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<tr>
<td>Rotor Resistance</td>
<td>0.006 pu</td>
</tr>
<tr>
<td>Rotor Leakage Reactance</td>
<td>0.086 pu</td>
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</table>

Table 7.10: RTDS Doubly Fed Induction Generator Step-Up Transformer and Saturation Parameters

<table>
<thead>
<tr>
<th>DFIG Step-Up Transformer Parameters</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Winding Configuration</td>
<td>Three Phase Y-y-y</td>
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<tr>
<td>LV1 Winding Voltage - DFIG Stator</td>
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</tr>
<tr>
<td>LV2 Winding Voltage - Power Converter</td>
<td>0.69 kV</td>
</tr>
<tr>
<td>HV Winding Voltage</td>
<td>23.9 kV</td>
</tr>
<tr>
<td>Rated Power</td>
<td>2.5 MVA</td>
</tr>
<tr>
<td>Rated Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>HV Winding Reactance</td>
<td>0.1 pu</td>
</tr>
<tr>
<td>LV1 Winding Reactance - DFIG Stator</td>
<td>0.1 pu</td>
</tr>
<tr>
<td>LV2 Winding Reactance - Power Converter</td>
<td>0.1 pu</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Saturation Characteristics Parameters</th>
<th></th>
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<tbody>
<tr>
<td>Slow Flux Time Constant</td>
<td>5 sec</td>
</tr>
<tr>
<td>Rated Power</td>
<td>0.833 MVA</td>
</tr>
<tr>
<td>Rated Voltage</td>
<td>0.4 kV</td>
</tr>
<tr>
<td>Rated Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Magnetizing Current (% Irated)</td>
<td>0.30%</td>
</tr>
<tr>
<td>Air Core Inductance</td>
<td>0.2 pu</td>
</tr>
<tr>
<td>Flux Knee Point</td>
<td>1.2 pu</td>
</tr>
<tr>
<td>Hysteresis Loop Width (%)</td>
<td>10%</td>
</tr>
</tbody>
</table>
CHAPTER EIGHT
CONTROLLER HARDWARE-IN-THE-LOOP RESULTS AND DISCUSSION

This chapter outlines the results of the controller hardware-in-the-loop experiments recorded and provides several key observations and interpretations with respect to the performance of the Hybrid Method. The flexibility and configurability of the Hybrid Method of performing fault ride-through evaluations has driven the need to limit the configuration options of the physical system, the voltage vector trajectories of the vector controller, and the fault voltage depth of the desired fault events, all in order to produce a manageable set of results that still represent the functionality and capabilities of the Hybrid Method.

In this work, only two voltage depths will be considered – 50% and 0% remaining voltage. This provides a good demonstrative balance between a ZVRT fault scenario, where voltage regulation is relatively easy because there is very little power involved, and an LVRT fault scenario, where there exists a fair amount of energy and voltage regulation becomes more difficult. Clearly the system can produce a nearly infinite number of different scenarios. The configuration options of the physical system are limited to the constraint that the series and shunt elements for each phase are not independently adjusted in any of the results. This means that the same series impedance is used on all three phases and the same shunt impedance is used on each of the faulted phases. Finally, the voltage trajectories of the feed-forward reference voltage control are limited to only scalar adjustments and no phase angle deviation is performed. Additionally, the pre-fault and post-fault times in which the series element is inserted into the circuit are rather short, one half of a second, in order to allow for the capture of a complete operation cycle of the Hybrid Method. In practice, these would be lengthened to allow for the
machine to recover from the slight transient produced by the insertion and removal of the series impedance.

This chapter will overview the overall performance of the embodiment of the Hybrid Method that has been presented in the previous chapters. Additionally, this chapter will demonstrate the ability of the Hybrid Method to insert very large series impedances with limited transients, the magnetic flux decoupling between the two transformers, a delayed voltage recovery will be shown where the series impedance limits the post fault voltage rise at the point of common coupling, and the one fault scenario that shows an inherent limitation based on the configuration limitations imposed on the Hybrid Method physical system.

**Controller Hardware-In-the-Loop Results**

A total of thirteen fault scenarios spanning both device under test models and all four fault types discussed in this work have been recorded and included in the appendices of this dissertation. Appendix C contains the vector controller timing parameters that pertain to all of the simulations. Appendices D through P contain the parameters specific to the fault scenario and the resulting waveforms from the fault scenario. Table 8.1 demonstrates the fault scenarios recorded and the specific appendix where the results can be found.

For each fault scenario evaluated, the following waveforms are provided in the results: the time series and phasor quantities of the voltages measured at the point of common coupling, the current into the point of common coupling from the DUT, the real and reactive power of the DUT measured at the point of common coupling, the electrical torque of the DUT, the current out of the power amplifier, the DC bus voltages of the power amplifier, the series bypass and
shunt fault switch states, the flux in the amplifier transformer, the magnetizing current of the amplifier transformer, the magnetizing current of the DUT transformer, the amplifier reference voltages output from the controller, and the feedback compensation voltage provided by the controller.

Many of the values demonstrated in these waveforms are plotted on a per unit scale. It is important to identify these scales such that the waveforms can be properly interpreted. All of the currents, with the exception of the transformer magnetizing currents, are on a 15 MVA base at 23.9 kV. As all of the transformers magnetizing branches are connected to the low voltage, secondary windings, the transformer magnetizing currents have per unit values calculated on the rated power of the transformer given the rated voltage of the low voltage windings. The per unit electrical torque of each machine is calculated on the base power of the machine given the rated frequency, which is 60 Hz for both machines. The vector controller per unit voltage is inherently calculated within the controller and is equivalent to the base voltage of the point of common coupling, which is 23.9 kV.
Table 8.1: The Results Collected and Their Associated Appendix Location for the CHIL Experiments

<table>
<thead>
<tr>
<th>Location</th>
<th>Machine Model</th>
<th>Fault Type</th>
<th>Remaining Voltage</th>
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</thead>
<tbody>
<tr>
<td>Appendix D.</td>
<td>Sync. Gen.</td>
<td>3PF</td>
<td>0%</td>
</tr>
<tr>
<td>Appendix E.</td>
<td>Sync. Gen.</td>
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<td>50%</td>
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<tr>
<td>Appendix F.</td>
<td>Sync. Gen.</td>
<td>3PF</td>
<td>0%-FIDVR</td>
</tr>
<tr>
<td>Appendix G.</td>
<td>Sync. Gen.</td>
<td>SLGF</td>
<td>0%</td>
</tr>
<tr>
<td>Appendix H.</td>
<td>Sync. Gen.</td>
<td>SLGF</td>
<td>50%</td>
</tr>
<tr>
<td>Appendix I.</td>
<td>Sync. Gen.</td>
<td>DLF</td>
<td>0%</td>
</tr>
<tr>
<td>Appendix J.</td>
<td>Sync. Gen.</td>
<td>DLF</td>
<td>50%</td>
</tr>
<tr>
<td>Appendix K.</td>
<td>Sync. Gen.</td>
<td>LLF</td>
<td>0%</td>
</tr>
<tr>
<td>Appendix L.</td>
<td>DFIG</td>
<td>3PF</td>
<td>0%</td>
</tr>
<tr>
<td>Appendix M.</td>
<td>DFIG</td>
<td>3PF</td>
<td>50%</td>
</tr>
<tr>
<td>Appendix N.</td>
<td>DFIG</td>
<td>SLGF</td>
<td>50%</td>
</tr>
<tr>
<td>Appendix O.</td>
<td>DFIG</td>
<td>DLF</td>
<td>50%</td>
</tr>
<tr>
<td>Appendix P.</td>
<td>DFIG</td>
<td>LLF</td>
<td>50%</td>
</tr>
</tbody>
</table>

Overall, the results demonstrated for each fault scenario evaluated coincide with what would be expected. Not demonstrated directly with these results is the repeatability of each fault scenario, which is only inhibited by the fact that the fault triggering signal assumes half-wave symmetry. The fault events recorded and presented in the appendices are taken after at least five consecutive runs without any significant deviation. Within the results, the current through the amplifier sometimes consists of transients above 1 pu. However, knowing that the power amplifier is capable of short term, 100 to 200 ms, of 200% overload, the values are well within the limitations of the power amplifier. The majority of these short term overloads are caused by the deceleration of the synchronous generator once the fault has cleared. More importantly, the voltage range of the DC bus in spite of these momentary overloads remains bounded by the power amplifier under-voltage and overvoltage limits.

Specifically demonstrated with the synchronous generator is the inherent current division built into the reactive divider network of the Hybrid Method physical system. The three phase
fault scenarios on the synchronous generator demonstrate that the asymmetrical, sub-transient current peaks of over 4.5 pu are effectively shunted away from the power amplifier. As demonstrated by the synchronous generator scenario resulting in Fault Induced Delayed Voltage Recovery (FIDVR), the Hybrid Method is able to maintain stability of the system and operate within the system constraints under the most severe situations. Also demonstrated here is the ability of the saturation block within the feedback voltage compensation loops and the ultimate saturation of the output reference voltage to limit the action of the Hybrid Method to maintain the operational limitations. The next sections will discuss in detail more of the specific observations of the performance of the Hybrid Method for fault ride-through evaluations.

Large Series Impedance Insertion on the Synchronous Generator

One of the most important aspects with respect to the successful implementation of the Hybrid Method is the capability of inserting and removing the series impedance with limited transient behavior while maintaining the voltage stability at the point of common coupling. To demonstrate this, a test scenario in which parametric uncertainty is intentionally included was created with the synchronous generator model delivering 10 MW to the point of common coupling. In this scenario, a series combination of a 5 ohm resistance and 100 mH reactance is inserted and removed without the creation of a fault. Additionally in this scenario, the impedance of the step-up transformer is purposely left out of the total series impedance when the series impedance is inserted in order to demonstrate the capabilities of the Hybrid Method to deal with parametric uncertainty. This scenario represents a very difficult task because the fault duty
from the amplifier to the point of common coupling is instantaneously changed from roughly 300 MVA to just under 15 MVA, or from 30 times the generator rating to just 1.5 times the rating.

Figure 8.1 demonstrates the phasor measurements of the phase voltages at the point of common coupling with the series impedance inserted at 0.2 s and then removed one second later at 1.2 s. The voltage drops from just above 1 pu, down to 0.95 pu when the series impedance is inserted. It then returns to the previous value after the impedance is removed. While all of the 5% voltage drop cannot be directly attributed to the impedance of the power amplifier step-up transformer and some additional parametric uncertainty must exist, both the voltage magnitude and phase remains flat and constant. It should be noted that this pre-fault voltage dip of 95% remaining voltage would still meet the IEC 61400-21 testing envelop found in Figure 2.2. Figure 8.2 illustrates the per unit currents of the device under test during this particular event. There exists some transient nature that cannot be completely eliminated given the magnitude of both the series impedance and the apparent power of the generator.

Figure 8.1: Synchronous Generator – 100 mH Reactance Series Impedance – The phasor measurements of the phase voltages at the point of common coupling.
Figure 8.2: Synchronous Generator – 100 mH Reactance Series Impedance – The generator line currents into the point of common coupling.

Figure 8.3 illustrates the active and reactive power delivered by the device under test during this test scenario. The active power contains a low frequency oscillation, since only very little damping of the generator exists and the reactive power demonstrates a step change with a slow decay. One important factor to notice here is that, given sufficient time, approximately twice the one second interval; the generator would again reach the original steady state operating point.

Figure 8.3: Synchronous Generator – 100 mH Reactance Series Impedance – The active and reactive power of the generator measured at the point of common coupling.
Figure 8.4 and Figure 8.5 demonstrate the phasor measurements of the power amplifier reference voltages and instantaneous feedback compensation voltage, respectively. The feedback compensation voltage clearly has an inherent step change when the series impedance is inserted and removed from the circuit that is directly contributed to the impedance calculation. However, the phasor measurements of the power amplifier reference voltages demonstrate more concisely how the Hybrid Method vector controller is responding to this large impedance step change because the feed-forward reference voltage is held constant during the entire simulation at 1 pu. The resulting changes in the power amplifier reference voltages are actually the feedback voltage compensation. From Figure 8.4, it is clear that the reference voltage is tracking both the low frequency oscillation of the active power and the ramp of the reactive power while the series impedance is in the circuit.

![Phasor Measurements of the Reference Voltages](image)

Figure 8.4: Synchronous Generator – 100 mH Reactance Series Impedance – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure 8.5: Synchronous Generator – 100 mH Reactance Series Impedance – The series voltage drop compensation calculated within the LabVIEW FPGA controller.

Once the series impedance is removed, the generator exhibits a near opposite response. This is significant given the fact that the fault duty of the circuit is returned to 30 times the generator rating and the feedback compensation voltage loop offers very little support. This indicates that the insertion of the series resistance has not dramatically affected the characteristics of the generator.

The test scenario presented here represents a significant result and accomplishment for the Hybrid Method, as the largest possible series impedance is capable of being inserted on machine that is delivering two thirds of the rated power of the Hybrid Method, while maintaining stability of the system. The results demonstrated in this work show that this amount of series impedance is never required given the feed-forward reference voltage control of the Hybrid Method vector controller. Nevertheless, it is an important achievement with respect to the design and implementation of the Hybrid Method of performing fault ride-through evaluations.
Another important design aspect of the Hybrid Method is the fact that, during a fault event, the magnetic flux of the power amplifier step-up transformer is decoupled from the magnetic flux of the device under test transformer. This is made possible by the fact that the series impedance electrically distances the fault created at the point of common coupling from the power amplifier and the step-up transformer. The most extreme test scenario that demonstrates this concept is a three phase fault with zero remaining voltage on the synchronous generator. This fault scenario represents the most strenuous condition because it has the most likelihood of a fault clearing voltage rise that is nearly 180° out of phase from where the fault was initialized. Figure 8.6 demonstrates the phasor measurements of the phase voltages at the point of common coupling for the three-phase fault with zero remaining voltage. Figure 8.7 illustrates the internal magnetic flux within the power amplifier step-up transformer.
Figure 8.6: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling. The fault is initiated at 0.6 sec and cleared at 0.7 sec.

Figure 8.7: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The flux within the power amplifier step-up transformer.

It can be seen in the magnetic flux waveforms that there exists some steady-state offset between the flux within each phase and they are not quite symmetrical about the axis. This is clearly evident during the fault event, just after 0.6 s. There are a number of possible reasons for this including: analog input and/or analog output bias between the RTDS and the FPGA.
controller or a response to the non-ideal DC bus voltages. This will be investigated fully in the future to determine the cause and formulate a resolution to this issue if it is found to be indicative of the real physical system. Nevertheless, the magnetic flux within the transformer does remain bounded and exhibits properties of attempting to be symmetrical about the axis by having considerable step changes in voltage result in nearly constant DC bias.

However, the magnetizing current drawn by both of the transformers in the system is of more importance. These magnetizing currents are shown for the power amplifier step-up transformer and the device under test transformer in Figure 8.8 and Figure 8.9, respectively. As was seen in the magnetic flux waveforms of the power amplifier transformer, phase B exhibits approximately a -5 Vs DC bias resulting in a deviation of the magnetizing current on phase B. This magnetizing current deviation represents only mild saturation of the power amplifier transformer. The current on phase B results in a maximum peak magnetizing current of only 15% of the rated transformer current.

Figure 8.8: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.
However, when examining the magnetizing current of the device under test transformer, the extent of magnetic saturation is severe, as illustrated by per phase magnetizing current peaks of 4 pu, 1.5 pu, and 0.5 pu based upon the transformers rated full load current. The highly non-linear magnetizing branch impedance represented by these currents can prove to be a difficult challenge for a device under test to handle with respect to control, electrical component ratings, and even mechanical stress as demonstrated by the electrical torque of the machine. The complete set of plots for this fault scenario can be found in Appendix D.

Three Phase Fault with a Delayed Voltage Recovery on the Synchronous Generator

The fault scenario presented in Appendix F. illustrates one method of creating a Fault Induced Delayed Voltage Recovery (FIDVR) [11] with this embodiment of the Hybrid Method. In this scenario, the series impedance is chosen to be larger than what is required for a nominal rectangular voltage dip and works to limit the voltage support achievable by the power amplifier. Figure 8.10 and Figure 8.11 demonstrate the phasor measurements of the phase voltage at the
point of common coupling and the phasor measurements of the power amplifier reference voltages during the fault.

![Phasor Measurements of the Voltage at the PCC](image1)

Figure 8.10: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The phasor measurements of the phase voltages at the point of common coupling.

![Phasor Measurements of the Reference Voltages](image2)

Figure 8.11: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
The phase voltage phasor measurements at the point of common coupling illustrated a sharp transition to zero voltage at 0.6 s and a recovery voltage of over 50% once the fault is released at 0.7 s and eventually cleared a few milliseconds later. After the fault is cleared, the voltage does not quickly return to the nominal voltage but instead is subjected to some low frequency oscillation as it ramps from the post fault voltage of just over 50% voltage back to nominal voltage over the next half of a second.

This is due to the series impedance being rather large and the feedback compensation voltage being saturated such that the power amplifier is only able to provide a limited amount of voltage support at the point of common coupling. This is evident in the phasor measurements of the power amplifier voltage references where the voltage magnitude is limited to 135% of the nominal voltage during the recovery period.

Although clearly possible as illustrated by this example, this method of emulating a FIDVR type fault scenario is not the most desirable or controllable way to create this type of event. Future work will develop a method of utilizing post fault time series recovery voltage profiles in order to adjust the feed-forward reference voltage. Coupling this with smaller series impedances that result in tighter voltage regulation to the reference voltage will provide a more controllable and reliable method of creating FIDVR events in the future.

**Single Line to Ground Fault on the Synchronous Generator**

The fault scenarios that subject the synchronous generator to single line to ground faults, found in Appendix G. and Appendix H. , illustrate a fundamental challenge associated with the application of the Hybrid Method as embodied in this work. Given that the synchronous
generator is connected to the point of common coupling through a step-up transformer that has delta wye vector group, the magnitude and phase of the fault voltages are transformed through the winding such that a completely different vector group is actually imposed upon the terminals of the generator. Given this vector transformation, a single line to ground fault at the point of common coupling actually results in fault voltages at the terminals of the generator that resemble a line-to-line fault. A more comprehensive study of the resulting vector transformations of fault voltages across the windings of various transformer winding configurations can be found in [57], where this is classified as a type C fault, a line-to-line fault, at the terminals of the generator.

Nevertheless, the underlying issue associated with this vector transformation of the fault voltages is that the fault current delivered by the generator is not proportional to the fault voltages created by the Hybrid Method. This greatly affects the current division inherent to the reactive divider network and can result in larger than expected current magnitudes. However, as will be demonstrated these currents are not outside the bounds of the power amplifier.

To demonstrate this challenge, the most severe example of this fault scenario is taken from Appendix G, where the synchronous generator is subjected to a single line to ground fault with zero remaining voltage. Figure 8.12 illustrates the phase voltage waveforms that indicate a single line to ground fault on phase B. Figure 8.13 demonstrates the fault current response of the generator as measured into the point of common coupling. Figure 8.14 illustrates the current measured out of the power amplifier at the high voltage terminals of the step-up transformer. It is evident that the response of the generator to the single line to ground fault is nearly equal fault currents delivered on phases A and B, but 180° out of phase from each other. The fact that these fault currents are seen on phases A and B corresponds directly to the transformer winding
connections. Unfortunately, the reactive divider network is only going to provide current division on the phase that is actively being shunted at the point of common coupling, phase B.

Figure 8.12: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The phase voltages measured at the point of common coupling. The fault occurs at 0.59 sec and clears at 0.71 sec.

Figure 8.13: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The generator line currents into the point of common coupling. The fault occurs at 0.59 sec and clears at 0.71 sec.
The fact that there is no current division on the un-faulted phases implies that the fault current being produced by the generator on phase A will be required to be absorbed by the power amplifier as demonstrated in the power amplifier currents. The fault current produced by the generator on phase A results in a 125% momentary overload on phase A of the power amplifier. However, this is easily within the momentary overload boundaries of the power amplifier and is not a cause for concern in this particular fault scenario. It should be reiterated that the 10 MVA synchronous generator represents a very large load with respect to the ratings of the Hybrid Method physical system and this challenge with fault voltage vector transformations is not problematic given the results presented.

Another impressive result in this scenario comes from the fact that the Hybrid Method vector controller is able to regulate the in-fault voltages. Even though the series impedance on phase A is the same as the other three phases and the fault current on phase A is transferred through this series impedance, the feedback compensation voltage loop is able to maintain sufficient regulation on the phase A voltage at the point of common coupling. This is demonstrated more clearly in Appendix G. by analyzing the controller response during the fault.
Summary

As demonstrated by the results presented in this section, the performance of the complete Hybrid Method meets the fundamental objective of reducing the fault duty required for fault ride-through evaluations. The design of the vector controller has been verified by presenting four types of faults, symmetrical and unsymmetrical, with varying fault voltage depth to two simulated devices under test. The feed-forward reference voltage control and the feedback compensation voltage control demonstrate, through these results, the ability to control the time-variant nature of the Hybrid Method physical system.

By constraining the configuration of the reactive divider network and vector controller reference trajectories to produce a reasonably sized data set, some of the more advanced features of the Hybrid Method are not able to be demonstrated in this dissertation. Such items include the capability of providing the natural power system response to faults by controlling the references on the un-faulted phases and the possibility of using time series voltage profiles once the fault has cleared to emulate a slow voltage recovery profile.
CHAPTER NINE
CONCLUSIONS

This dissertation has presented the design and analysis of a Hybrid Method of performing fault ride-through evaluations on multi-megawatt, medium voltage power conversion equipment. The Hybrid Method successfully couples the two existing technologies together, namely a reactive voltage divider network and a power electronic variable voltage source, in order to reduce the short circuit duty required for implementation. The background understanding of this limitation with respect to the existing technologies has been presented and demonstrates that the Hybrid Method is a justifiable way to minimize the fault duty required for fault evaluations. The Hybrid Method has also shown the capabilities to both regulate the in-fault voltage and decouple the magnetic flux within the two transformers in the system for both symmetrical and unsymmetrical faults.

The physical system, control objectives, and operation cycle of the Hybrid Method have been analyzed with respect to the overall objective of reducing the fault duty of the system. The Hybrid Method vector controller has been designed to control the time-variant nature of the Hybrid Method operation cycle, limit the fault current seen by the power electronic variable voltage source, and provide regulation of the fault voltage at the point of common coupling with the device being evaluated.

The operation of both the Hybrid Method physical system and vector controller has been verified through controller hardware-in-the-loop experiments that have been created in order to simulate the physical system in real-time against the prototype implementation of the vector controller. A detailed model of the physical system has been simulated in a Real Time Digital Simulator and is controlled with the Hybrid Method vector controller implemented on a National
Instruments FPGA. In order to evaluate the complete performance of the Hybrid Method with respect to varying device under test characteristics, both a synchronous generator and a doubly fed induction generator have been modeled as the device under test with the simulations of the Hybrid Method’s physical system. Finally, the results of the controller hardware-in-the-loop experiments have been presented to demonstrate that the Hybrid Method, is a viable solution to performing fault ride-through evaluations on multi-megawatt, medium voltage power conversion equipment.

Future Work

Throughout this dissertation, items have been noted for future work with respect to the development, implementation, and simulation of the Hybrid Method. The following tasks illustrate the continuing development of the Hybrid Method with respect to both the refinement of the simulated system and the practical implementation within the larger scope of the Hardware-In-the-Loop Grid Simulator project.

The Hybrid Method Physical System and Reactive Divider Network Configuration:

- Map the complete frequency dependent impedance of the series and shunt snubber circuits given the variable impedances of both the series and shunt impedances.
- Implement configurations of the reactive divider network that are able to account for the apparent issues associated with phase shifting transformers.

The Hybrid Method Vector Control Implementation:

- Optimization of the gains for the SOGI filters and implementation of variable frequency capabilities within the SOGI filters.
• Develop a precise, variable frequency, reference generator for the feed-forward reference voltage control.

• Implement post fault time series recovery voltage profiles into the feed-forward regulation voltage control.

Controller Hardware-In-the-Loop Experiments:

• Further investigate the optimum time domain, large or small time step, for the reactive divider network given the parasitic impedances created by the reactive divider model. Investigate the root cause of the steady state power amplifier transformer flux offset and provide compensation through the controller if required.
APPENDICES
Appendix A. National Instruments LabVIEW Virtual Instruments

This Appendix contains the front panels and block diagrams for the important HMI and FPGA Vis. The HMI VI contains the user interface, the MODBUS TCP/IP communication, FPGA initialization and parameterization. In communicating the reactive divider network settings to the RTDS through MODBUS registers the control word outlined in Table A.1 is used to signify the individual switch states for each phase.

Table A.1: The Reactive Divider Network per Phase 20-Bit Configuration Word

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<th>Bit Label</th>
<th>Bit Position</th>
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<th>Bit Value</th>
<th>Description</th>
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<td>Series Res. Tap 0</td>
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<td>2</td>
<td>Series Res. Tap 1</td>
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<tr>
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<td>2</td>
<td>4</td>
<td>Series Res. Tap 2</td>
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<tr>
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<td>3</td>
<td>8</td>
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Figure A.1: The LabVIEW front panel Human Machine Interface (HMI) of the Hybrid Method.
Figure A.2: The main processing loop for the front panel of the HMI for the Hybrid Method

Figure A.3: The secondary processing loop to send parameters from the HMI to the FPGA.

Figure A.4: The TCP MODBUS processing loop of the HMI to communicate with the RTDS.
Figure A.5: The HMI sub VI that computes the continuous SOGI transfer functions and then converts them to discrete fixed point representations.
Figure A.6: The HMI sub VI that calculates the Reactive Divider Network 20 bit configuration word for MODBUS communication to RTDS.

Figure A.7: The HMI sub VI that uses the controls from the front panel to calculate the series impedance values in both floating point for display on the front panel and fixed point representations to be passed down to the FPGA DSP Loop.
Figure A.8: The FPGA front panel. The controls on this front panel are the only method communication with the HMI.
Figure A.9: The FPGA initialization routine that loads the fixed point representations of the SOGI filters into block memory and initializes the Boolean states of the DSP loop.

Figure A.10: The simple state machine of the Hybrid Method implemented on the FPGA.

Figure A.11: The FPGA sub processing loop that receives requests to solve the SOGI transfer functions on a FIFO and output completed requests on another FIFO. The FIFOs contain the block memory address SOGI transfer function to be solved.
Figure A.12: The FPGA DSP loop that implements the vector control algorithm.
Figure A.13: The FPGA sub VI utilized to solve the fixed point SOGI transfer functions. This is a modified NI VI that allows for the internal states to be stored to block memory.

Figure A.14: The FPGA sub VI that calculates the feedback compensation voltage. The discrete difference of the input current is calculated to calculate the quadrature signal and then the complex multiplication by the series impedance is performed.
Figure A.15: The FPGA sub VI that determines the zero crossing of particular signals by determining if the sign of the signal has changed.

Figure A.16: The FPGA sub VI that creates the saw tooth signals that indicate the angle of the present signal based off of the zero crossings.
Appendix B. Real Time Digital Simulator RSCAD Model Images

This appendix contains the RSCAD block diagrams of the simulations run in the RTDS. The detailed parameters for these models can be found in Chapter 7 when the real-time digital simulation of the Hybrid Method physical system is discussed. Besides simulation block diagram shown in Figure B.1, all of the other block diagrams are simulated in the small time step domain in order to increase the overall fidelity of the model. The only items simulated in the large time step domain are Active Front Ends, general controls for the DUT, and the analog and digital input and output.

![Image](image-url)

Figure B.1: Combination of the two RSCAD subsystems, one for each rack, that are included in the RTDS model of the Hybrid Method physical system.
Figure B.2: The small time step model of a single-phase of the power amplifier output coupled to the single phase step-up transformer and connected to the reactive divider network for the particular phase.
Figure B.3: The small time step single-phase reactive divider network RSCAD model.
Figure B.4: The single-phase voltage oriented control and lineary physical system model of the active front ends that produces the DC bus voltage for the single-phase power amplifier output stage.
Figure B.5: The small time step model of the synchronous generator used to verify the performance of the Hybrid Method.

Figure B.6: The small time step model of the doubly fed induction generator wind turbine generator used to verify the performance of the Hybrid Method.
Appendix C. Fault Ride-Through Results Parameters and Details

Table C.1 contains the vector control timing parameters for the simulation results recorded in appendices D through P. In this work, only two voltage depths will be considered, 50% and 0% remaining voltage. This provides a good balance between a ZVRT fault scenario, where voltage regulation is relatively easy because there is very little power involved at the point of common coupling, and an LVRT fault scenario where there exists a fair amount of energy and voltage regulation becomes more difficult. The configuration options of the physical system are limited to the constraint that the series and shunt elements for each phase are not independently adjusted in any of the results. This means that the same series impedance is used on all three phases and the same shunt impedance is used on each of the faulted phases. Finally, the voltage trajectories of the feed-forward reference voltage control are limited to only scalar adjustments and no phase angle deviation is allowed.

Table C.1: The Vector Control Timing Parameters for all of the Results Recorded.

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<td>Shunt FIRE Delay</td>
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<td>Shunt OFF Delay</td>
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<tr>
<td>Fault Duration</td>
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<td>Post-Fault Delay Time</td>
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<td>Fault Duration</td>
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<td>Post-Fault Delay Time</td>
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Appendix D. Synchronous Generator – Three Phase Fault, 0\% Remaining Voltage

Table D.1: Fault Parameters – SG – 3PF – 0\% Remaining Voltage

<table>
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<th>Parameter</th>
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<th>Phase B</th>
<th>Phase C</th>
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Figure D.1: Synchronous Generator – Three Phase Fault, 0\% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure D.2: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure D.3: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The generator line currents into the point of common coupling.
Figure D.4:  Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure D.5:  Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure D.6: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The electrical torque of the generator.

Figure D.7: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure D.8: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure D.9: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure D.10: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure D.11: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure D.12: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure D.13: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure D.14: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix E. Synchronous Generator – Three Phase Fault, 50% Remaining Voltage

Table E.1: Fault Parameters – SG – 3PF – 50% Remaining Voltage

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<th>Parameter</th>
<th>Phase A</th>
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<th>Phase C</th>
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<tr>
<td>Tapped Series Inductance (mH)</td>
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<td>Neutral Switch</td>
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Figure E.1: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure E.2: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure E.3: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The generator line currents into the point of common coupling.
Figure E.4: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure E.5: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure E.6: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The electrical torque of the generator.

Figure E.7: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure E.8: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure E.9: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure E.10: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure E.11: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure E.12: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure E.13: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure E.14: Synchronous Generator – Three Phase Fault, 50% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix F.  Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery

Table F.1:  Fault Parameters – SG – 3PF – 0% Remaining Voltage – FIDVR

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
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<tbody>
<tr>
<td>Tapped Series Resistance (Ohms)</td>
<td>5</td>
<td>5</td>
<td>5</td>
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<tr>
<td>Tapped Series Inductance (mH)</td>
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<tr>
<td>Fixed Series Inductance (mH)</td>
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<td>50</td>
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<tr>
<td>Fixed Shunt Inductance (mH)</td>
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<td>0</td>
</tr>
<tr>
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<td>10000</td>
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<td>Feedback Saturation (%V)</td>
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<tr>
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</tr>
<tr>
<td>Neutral Switch</td>
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Figure F.1:  Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The phase voltages measured at the point of common coupling.
Figure F.2: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The phasor measurements of the phase voltages at the point of common coupling.

Figure F.3: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The generator line currents into the point of common coupling.
Figure F.4: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure F.5: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The active and reactive power of the generator measured at the point of common coupling.
Figure F.6: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The electrical torque of the generator.

Figure F.7: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure F.8: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The switch states of the series bypass and shunt fault switches.

Figure F.9: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The flux within the power amplifier step-up transformer.
Figure F.10: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The magnetizing current of the power amplifier step-up transformer.

Figure F.11: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The magnetizing current of the synchronous generator step-up transformer.

Figure F.12: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure F.13: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure F.14: Synchronous Generator – Three Phase Fault, 0% Remaining Voltage, Delayed Voltage Recovery – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix G. Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage

Table G.1: Fault Parameters – SG – SLGF – 0% Remaining Voltage

<table>
<thead>
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<th>Parameter</th>
<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
</tr>
</thead>
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<td>Tapped Series Inductance (mH)</td>
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<td>Fixed Shunt Inductance (mH)</td>
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<td>Feedback Saturation</td>
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<td>10000</td>
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<td>Feedback Saturation (%V)</td>
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<tr>
<td>Shunt Switches Operated</td>
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<td>Neutral Switch</td>
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Figure G.1: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure G.2:  Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure G.3:  Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The generator line currents into the point of common coupling.
Figure G.4: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure G.5: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure G.6: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The electrical torque of the generator.

Figure G.7: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure G.8: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure G.9: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure G.10: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure G.11: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure G.12: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure G.13: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure G.14: Synchronous Generator – Single Line to Ground Fault, 0% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix H. **Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage**

Table H.1: Fault Parameters – SG – SLGF – 50% Remaining Voltage

<table>
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<tr>
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<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
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<tbody>
<tr>
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<td>Neutral Switch</td>
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Figure H.1: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure H.2:  Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure H.3:  Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The generator line currents into the point of common coupling.
Figure H.4: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure H.5: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure H.6: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The electrical torque of the generator.

Figure H.7: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure H.8: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure H.9: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure H.10: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure H.11: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure H.12: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure H.13: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure H.14: Synchronous Generator – Single Line to Ground Fault, 50% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix I. Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage

Table I.1: Fault Parameters – SG – DLGF – 0% Remaining Voltage

<table>
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<tr>
<th>Parameter</th>
<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
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<td>Tapped Series Resistance (Ohms)</td>
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<td>Feedback Saturation (%V)</td>
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<td>Neutral Switch</td>
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Figure I.1: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure I.2: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure I.3: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The generator line currents into the point of common coupling.
Figure I.4: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure I.5: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure I.6: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The electrical torque of the generator.

Figure I.7: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure I.8: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure I.9: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure I.10: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure I.11: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure I.12: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure I.13: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure I.14: Synchronous Generator – Double Line to Ground Fault, 0% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix J.  Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage

Table J.1:  Fault Parameters – SG – DLGF – 50% Remaining Voltage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tapped Series Resistance (Ohms)</td>
<td>5</td>
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<tr>
<td>Tapped Series Inductance (mH)</td>
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<td>Fixed Shunt Inductance (mH)</td>
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<td>Feedback Saturation (%V)</td>
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<td>Neutral Switch</td>
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Figure J.1:  Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure J.2: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure J.3: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The generator line currents into the point of common coupling.
Figure J.4: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure J.5: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure J.6: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The electrical torque of the generator.

Figure J.7: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure J.8: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure J.9: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure J.10: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure J.11: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure J.12: Synchronous Generator – Double Line to Ground Fault, 50% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix K.  Synchronous Generator – Line to Line Fault, 0% Remaining Voltage

Table K.1:  Fault Parameters – SG –LLF – 0% Remaining Voltage

<table>
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<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
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</thead>
<tbody>
<tr>
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<tr>
<td>Tapped Series Inductance (mH)</td>
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<td>Fixed Series Inductance (mH)</td>
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</tr>
<tr>
<td>Fixed Shunt Inductance (mH)</td>
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<td>0</td>
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<tr>
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<tr>
<td>Shunt Switches Operated</td>
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<td>Neutral Switch</td>
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Figure K.1:  Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure K.2:  Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure K.3:  Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The generator line currents into the point of common coupling.
Figure K.4: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure K.5: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure K.6: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The electrical torque of the generator.

Figure K.7: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure K.8: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure K.9: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure K.10: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure K.11: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure K.12: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure K.13: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure K.14: Synchronous Generator – Line to Line Fault, 0% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix L. Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage

Table L.1: Fault Parameters – DFIG – 3PF – 0% Remaining Voltage

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<tr>
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<th>Phase A</th>
<th>Phase B</th>
<th>Phase C</th>
</tr>
</thead>
<tbody>
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<td>Tapped Series Resistance (Ohms)</td>
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<td>Feedback Saturation (%V)</td>
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<tr>
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<td>Neutral Switch</td>
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Figure L.1: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure L.2: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure L.3: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The generator line currents into the point of common coupling.
Figure L.4: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure L.5: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure L.6: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The electrical torque of the generator.

Figure L.7: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure L.8: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure L.9: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure L.10: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure L.11: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure L.12: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure L.13: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure L.14: Doubly Fed Induction Generator – Three Phase Fault, 0% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix M. Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage

Table M.1: Fault Parameters – DFIG – 3PF – 50% Remaining Voltage

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<tr>
<td>Fixed Shunt Inductance (mH)</td>
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<tr>
<td>Feedback Saturation (%V)</td>
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<td>39.53</td>
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<tr>
<td>Shunt Switches Operated</td>
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<td>X</td>
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<td>Neutral Switch</td>
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Figure M.1: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure M.2: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure M.3: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The generator line currents into the point of common coupling.
Figure M.4: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure M.5: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure M.6: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The electrical torque of the generator.

Figure M.7: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure M.8: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure M.9: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure M.10: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure M.11: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure M.12: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure M.13: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure M.14: Doubly Fed Induction Generator – Three Phase Fault, 50% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix N. Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage

Table N.1: Fault Parameters – DFIG – SLGF – 50% Remaining Voltage

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<th>Phase A</th>
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<th>Phase C</th>
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<tr>
<td>Tapped Series Resistance (Ohms)</td>
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<td>5</td>
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<tr>
<td>Tapped Series Inductance (mH)</td>
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<tr>
<td>Fixed Series Inductance (mH)</td>
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<td>Fixed Shunt Inductance (mH)</td>
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<td>Feedback Saturation (%V)</td>
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<td>Shunt Switches Operated</td>
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<td>Neutral Switch</td>
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Figure N.1: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure N.2: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure N.3: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The generator line currents into the point of common coupling.
Figure N.4: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure N.5: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure N.6: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The electrical torque of the generator.

Figure N.7: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure N.8: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure N.9: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure N.10: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure N.11: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure N.12: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure N.13: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure N.14: Doubly Fed Induction Generator – Single Line to Ground Fault, 50% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix O. Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage

Table O.1: Fault Parameters – DFIG – DLGF – 50% Remaining Voltage

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<th>Phase A</th>
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Figure O.1: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The phase voltages measured at the point of common coupling.

255
Figure O.2: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure O.3: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The generator line currents into the point of common coupling.
Figure O.4: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure O.5: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure O.6: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The electrical torque of the generator.

Figure O.7: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure O.8: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure O.9: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure O.10: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure O.11: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure O.12: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure O.13: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure O.14: Doubly Fed Induction Generator – Double Line to Ground Fault, 50% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
Appendix P. Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage

Table P.1: Fault Parameters – DFIG – LLF – 0% Remaining Voltage

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<th>Phase A</th>
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<td>Neutral Switch</td>
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Figure P.1: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The phase voltages measured at the point of common coupling.
Figure P.2: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The phasor measurements of the phase voltages at the point of common coupling.

Figure P.3: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The generator line currents into the point of common coupling.
Figure P.4: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The line currents measured out of the high voltage windings of the power amplifier step-up transformer.

Figure P.5: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The active and reactive power of the generator measured at the point of common coupling.
Figure P.6:  Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The electrical torque of the generator.

Figure P.7:  Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The DC bus voltages simulated using a linear approximation of the active front end for each of the three phases.
Figure P.8: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The switch states of the series bypass and shunt fault switches.

Figure P.9: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The flux within the power amplifier step-up transformer.
Figure P.10: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The magnetizing current of the power amplifier step-up transformer.

Figure P.11: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The magnetizing current of the synchronous generator step-up transformer.

Figure P.12: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The power amplifier reference modulation signals generated by the LabVIEW FPGA controller.
Figure P.13: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The phasor measurements of the power amplifier reference modulation signals generated by the LabVIEW FPGA controller.

Figure P.14: Doubly Fed Induction Generator – Line to Line Fault, 0% Remaining Voltage – The series voltage drop compensation calculated within the LabVIEW FPGA controller.
REFERENCES


