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A Voltage Flicker Suppression Device for Residential Air Conditioners and Heat Pumps

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A VOLTAGE FLICKER SUPPRESSION DEVICE FOR RESIDENTIAL AIR
CONDITIONERS AND HEAT PUMPS

A Thesis
Presented to
the Graduate School of
Clemson University

In Partial Fulfillment
of the Requirements for the Degree
Master of Science
Electrical Engineering

by
John Curtiss Fox
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Accepted by:
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ABSTRACT

In some circumstances, voltage flicker due to the inrush current of residential heat pump can be visible to the residents as a slight flashing of the household's lights during the compressor starting event. The voltage flicker problem is caused by contributions from both the equivalent power system impedances and the considerable inrush currents drawn by compressors. While this is not a new problem, and there are technologies on the market that attempt to alleviate the voltage flicker issue by decreasing the starting time of the compressor, no present solution attempts to correct for the problem at its root cause.

This thesis presents a device designed to utilize the time-proven method of using shunt capacitance for voltage correction and dynamically adapt it to the voltage flicker event by, in essence, learning the amount of capacitance needed to correctly compensate the voltage and virtually eliminate any flicker. The voltage flicker suppression device is aimed at being a one-size-fits-all, cost effective solution for not only new installations, but one that can be easily retrofit to existing HVAC installations where voltage flicker is an issue.

To better understand the challenges and requirements that such a device can be confronted with, background information is presented to address the characteristics of residential heat pump and their compressors, as well as contributing factors from residential power services. A human factors flicker study was conducted to experimentally determine the threshold of visible flicker and thus derive the level of voltage compensation required of the device.

The laboratory results presented in this thesis will demonstrate that, with no prior knowledge of the compressor or power system characteristics, the voltage flicker suppression device is capable of adapting to the required capacitance needed to ensure that the voltage flicker is corrected and the visible light flicker is minimized.

There are several limitations in terms of voltage compensation abilities that must be overcome when deciding the electrical location and controller characteristics of the device while maintaining the cost effectiveness of the solution. A discussion of these limitations is conducted in order to demonstrate the continuing work required for the device to ultimately meet the design goals.

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CHAPTER ONE

INTRODUCTION

This thesis presents a new voltage flicker suppression device that attempts to completely eliminate the visible voltage flicker caused by the starting event of a residential heat pump. While the term “flicker” is used to describe the actual change in luminance of the light source, it has become common terminology to refer to the voltage fluctuations that cause this lamp flicker as “voltage flicker” or just simply “flicker.” This thesis will use both voltage flicker and voltage fluctuation as interchangeable synonyms to refer to the cause of the actual lamp flicker.

Although there are already technologies on the market used to alleviate the voltage flicker issue, the device presented in this thesis is designed to correct for the voltage flicker at the source of the problem. In this introductory chapter, the background information necessary for understanding and interpreting the requirements and desired characteristics of a voltage flicker suppression device will be presented.

First, the motivation for this research is discussed, followed by a presentation of the various residential heat pump configurations, compressor traits, and residential power service characteristics as they relate to voltage flicker and voltage correction. An overview of the presently used voltage flicker standards and flicker suppression technology is offered, while the discussion is begun on how a new device will compensate for voltage flicker.

Motivation

At some point, nearly everyone has seen voltage flicker caused by the starting of a residential heat pump. In many residences, the voltage fluctuation of a starting compressor motor is of an acceptable value and does not cause an annoyance to the occupants or interfere with sensitive electronic equipment. Nevertheless, in some situations, the voltage flicker can be quite irritable to the occupants and possibly damaging to sensitive electronic equipment.

The problem of voltage flicker is generally more common in situations where a large single heat pump is used for an entire residence instead of two smaller units. This is rather common practice due to the cost effectiveness of a single unit. However, the compressor motor required for a large single unit will be almost twice the rated power in comparison to the smaller units, and this is where the issue of voltage flicker typically arises.

A compressor motor draws a large amount of inrush current, on average approximately five times the normal operating current. Depending on the characteristics of the power utility's distribution system, the size of the transformer and secondary conductors used, the voltage drop seen in the residence due to the compressor inrush current can be substantial. Figure 1.1 demonstrates the voltage drop due to the inrush current of a starting heat pump compressor.

There is much contention between heating ventilation and air conditioning (HVAC) manufacturers and power utilities as to who is to blame for the apparent voltage

drop [1]. From the point of view of the HVAC manufacturers, there are no current standards that limit the amount of inrush current that can be drawn, and it is actually the power utilities problem since their system is not designed to handle the inrush current. The power utilities stance is that the HVAC manufacturers are allowing for an unreasonable amount of inrush current, and sizing their equipment for an inrush event is not an optimum utilization of their resources.

Figure 1.1. Typical Heat Pump Inrush Event Including RMS Voltage and Current [2].

However, it is generally the power utilities that hear complaints about voltage flicker from customers because it is a perceived problem with their service. In response to a complaint, the power utility has limited options, and normally attempts to address the voltage flicker problem with a torque assist device, or hard-start kit, that will drastically shorten the length of the inrush current by starting the compressor motor faster.

Sometimes this is enough, but sometimes the voltage flicker is still present. At either rate, a torque assist device does not address the root of the problem and attempts to alleviate the issue by masking it.

To correctly address the root cause of the problem, shunt capacitance can be used in parallel with the starting motor compressor to dynamically compensate the voltage during starting. This thesis presents a voltage flicker suppression device (VFS) that is capable of recognizing the starting inrush current of a compressor and supplying the correct amount of shunt capacitance during the starting event to virtually eliminate the visible flicker.

The design goals for the VFS include having a one-size-fits-all device that is flexible enough to be retrofit alongside almost any heat pump compressor while not interfering or intruding on the current heat pump installation. This means that the device is separate from any currently installed HVAC equipment, and will not interfere with its present operation in any way. To be a one-size-fits-all design, the device should be able to adapt to the correct amount of voltage compensation at a particular installation by learning the correct amount of shunt capacitance needed to correct the voltage.

Another design goal is to make the device as cost effective as possible to ensure a certain market share, with a target price of under \$150 US per unit. This cost constraint has influenced several aspects of the VFS where better technology may exist but is not necessarily worth the added expense given the performance of the VFS.

Residential Air Conditioners and Heat Pumps

Residential heating, ventilation, and air conditioning (HVAC) equipment is generally separated into two distinct functional categories: air conditioners and heat pumps. While an air conditioner is technically a heat pump, the construction of an air conditioner allows only for heat transfer from the interior of a residence to the outside environment. Air conditioning only devices are typical installed in situations where heating is performed by alternative means, be it oil, natural gas, or electric.

A heat pump, on the other hand, allows for heat transfer in both directions and is more common in temperate climates. Heat pumps are sometimes equipped with auxiliary electric resistive heat strips to provide heating if an insufficient amount of heat can be extracted from the outside environment. The auxiliary heat is typically turned on by the thermostat after sufficient time has been given to the heat pump to attempt to meet the temperature set point. In special circumstances, the auxiliary heat may be turned on before, or even without, the heat pump.

The construction of both air conditioners and heat pumps consist of a compressor, a condensing coil, an evaporator coil, and expansion valve. Both heat pumps and air conditioners can be installed as either a package unit or a split system unit. A split system is separated into an air handler and a condensing unit. The air handler is installed inside the residence and typically houses the evaporator coil, expansion valve, and interior fan. If auxiliary heat is present, it is located in series with the evaporator coil with respect to air flow. The condensing unit is mounted in the outside environment and

contains the compressor, condensing coil, and external fan. A package unit consists of both the air handler and condensing unit within the same enclosure that is mounted external to the residence. Package unit heat pumps are commonly available with auxiliary heat as an option.

Figure 1.2. A Diagram of the General Layout of Residential Heat Pumps. [2]

Residential air conditioners and heat pumps typically consist of three electric motors: two fan motors and the compressor motor. The interior fan motor is used to circulate the air throughout the interior of the residence and over the evaporator coil, while the external fan motor is used to promote heat transfer with the condensing coil and the outside environment. The interior fan motor is generally rated for two to three times the power of the external fan motor since the interior fan moves a much larger volume of air. However, both fan motors are normally rated in the fractional horse power range.

The compressor motor is on average significantly larger than either fan motor. For example, a 5-ton heat pump may have a five horsepower compressor while both fan

motors are less than one horsepower each. The compressor motor's size causes the inrush current for larger units to be over half the rated capacity of the typical residential power service, which will inherently cause a large voltage drop during starting if the system impedance is relatively high.

Residential air conditioners and heat pumps are rated in two distinct ways, capacity and efficiency. The capacity of heat transfer in a heat pump is measured in tons, with a ton being equal to 12,000 Btu/hour. Thus a 2.5-Ton heat pump can effectively transfer 30,000 Btu's per hour. The efficiency of a heat pump is measured by one of two standards, the seasonal energy efficiency ratio (SEER) or just energy efficiency ratio (EER). The SEER rating is typical used on both air conditioners and heat pumps and takes into account the efficiency of a system over a range of expected temperatures. The EER rating is applicable only to air conditioners and is a measure of the efficiency for operation with an outside temperature of 95 degrees Fahrenheit. Both the SEER and EER ratings are the measure of a complete system efficiency given the specific combination of an air handler and condensing unit.

HVAC Compressor Characteristics

The type of compressors used for refrigeration applications are generally positive displacement single or multistage centrifugal compressors. These units consist of screw, reciprocating, rotary, or scroll designs constructed in open, semi-hermetic or hermetic enclosures. For the application of residential heat pumps, reciprocating and scroll

compressors are used almost exclusively. These compressors are designed with the motor and compressor in a common, hermetic, factory-sealed enclosure.

Practically all compressors used in residential applications on the US market are single-phase induction motors (SPIM) because the normal residential power service is single phase. The design of almost all SPIM can be broken down into two parts: the main (run) winding and the auxiliary (start) winding. Because the motor is single phase, the main winding alone has zero starting torque due to the equally balanced rotating fields seen by the rotor. The auxiliary winding is wound mechanically offset to the main winding in series with either a resistor or capacitor to electrically offset the magnetic field of the winding with respect to that of the main winding. The main winding in conjunction with the auxiliary winding produce a rotating field on the rotor that creates a starting torque and allows for acceleration. The direction of rotation can be changed by reversing the polarity of either the main or auxiliary winding. Depending on the desired running characteristics of the motor, the auxiliary winding may be removed after starting by a relay or centrifugal switch.

There are four main types of SPIMs with the starting torque and running efficiency needed for single-phase compressor applications: resistive start with induction run, capacitor start with induction run, capacitor start with capacitor run, or permanent split capacitor. The most commonly used SPIM is the permanent split capacitor (PSC) because of its increased operational efficiency and highly reliable design.

The PSC SPIM utilizes a single run capacitor in series with the auxiliary winding during both starting and running. The design of a PSC SPIM does not allow for a high

amount of starting torque since the capacitor is sized for running efficiency and is used in compressor applications where the system is able to self-equalize the pressure across the compressor. The equalized pressure allows it to start with no load and is typically accomplished with a capillary tube that connects both the high and low pressure sides of the compressor.

The design of a PSC SPIM does allow for the addition of torque assist devices, or hard-start kits, which can dramatically increase the starting torque of the motor and thus reduce the amount of time the motor spends in a locked rotor condition. A torque assist device may be required to start the compressor in a reasonable amount of time if a specific installation has a low nominal voltage or high system impedance.

Figure 1.3. A Diagram Demonstrating a Permanent Split Capacitance Single Phase Induction Motor's Main and Auxiliary Windings, as well as the Run Capacitance

Residential Power Service Characteristics

From the electric utilities distribution system, to the size of the conductors between the compressor and the breaker panel, there is no mistaking that the residential

power system characteristics play the largest role in the voltage flicker created by the inrush current of a compressor. There is currently no ANSI, NEC, IEEE, or other standard that places limitations on the inrush current for electrical equipment during startup. This leaves electric utilities to develop their own standards to deal with inrush current in terms of transformer and conductor sizing for residential circuits. These standards can differ to a large extent from utility to utility.

The layout of a residential service can vary greatly from location to location. For instance, in rural areas a residence is typically fed from a dedicated transformer, while in suburban and urban areas it is not uncommon for multiple residences to be fed from a single transformer. Many utilities' in-house standards place limitations on the amount of voltage flicker any one residence can cause to adjacent customers, but may or may not have a standard for the amount of voltage flicker the customer can cause to themselves.

Utilities will commonly recommend a torque assist device when confronted with a customer that is experiencing abnormally large voltage drop due to inrush current. However, the utility has only two options to directly reduce the voltage drop at the customer's service entrance, neither of which is an optimum utilization of a utility's time or distribution assets. Upsizing of the distribution transformer can decrease the voltage drop across the transformer for a given inrush current, but will increase the utility's losses due to the increased transformer core losses. A utility might elect to increase the size of the transformer secondary conductors in an effort to reduce the voltage drop between the transformer and the customer's service entrance. This can prove to be extremely costly if

underground cables are used. Neither option alone is guaranteed to completely resolve a customer's concerns if applied within practical limitations.

Figure 1.4 demonstrates the various impedances associated with a residential power service. The Thevenin impedance at the primary side of the distribution transformer is typically not a problem except for special circumstances in which the utilities distribution system is notably soft. As mentioned before, the impedance of the transformer and the feeder conductors can play heavily into the voltage drop.

The impedance of the conductors between the panel and the compressor motor can play a role in lengthening the starting time of the compressor motor. If these conductors are strictly sized for the steady state current, they may allow for significant voltage drop during starting. This will force the compressor to start with an even lower voltage, reducing the starting torque of the motor and increasing the time spent in a locked rotor condition.

Figure 1.4. The Impedance Breakout of a Typical Residential Power Service [2].

For the purpose of this project, it is not of concern where in the distribution system the largest amount of voltage drop occurs with respect to the desired amount of voltage correction. The impedance that is of issue is the equivalent Thevenin impedance seen at the breaker panel. A previous study, reported in [2], took numerous measurements of the impedance seen at the meter base of residences in an effort to determine the effects of the distribution system on voltage flicker. The results of this study included the low, average, and high values of impedances measured from line to line at the customer's meter base. The impedances are given in Table 1.1.

Table 1.1 Impedance values measured from line to line at the meter base [2].

Low (Stiff)	Average	High (Weak)
$0.019 + i0.038 \Omega$	$0.055 + i0.033 \Omega$	$0.135 + i0.093 \Omega$

The X/R ratio of the impedance as well as the magnitude will play a large role in the amount of shunt capacitance required to eliminate the voltage flicker. These impedance values do not include the entrance cables from the meter base to the panel or the conductor impedance from the panel to the compressor. It is expected that the X/R ratio at the panel and compressor will be increasingly lower than that of the meter base due to the relatively low inductance of these conductors. The impedance between the point of voltage compensation and the breaker panel will play a large role in the desired correction level because it is the voltage at the breaker panel that causes voltage flicker through the rest of the residence's circuits.

Current Flicker Suppression Technology

The current method of dealing with voltage flicker in residential applications is to install a torque assist device, or hard-start kit, on the offending compressor. Torque assist devices are recommended by HVAC manufacturers to reduce the starting time of the compressor if voltage flicker is an issue.

These torque assist devices are connected in parallel with original run capacitor of the PSC SPIM and consist of a positive temperature coefficient (PTC) thermistor in series with a capacitor. The PTC thermistor acts as a relay of sort for the torque assist device by effectively removing the torque assist capacitor from the circuit with a high series resistance. The capacitance of a torque assist device is generally much larger than that of the original run capacitor and the increased capacitance amplifies the magnetic field created by the auxiliary winding, thus increasing the starting torque of the motor.

This method does not actually address the root of the problem which is high system impedance. It simply reduces the time the compressor is in a locked rotor condition, shortening the length of the voltage flicker event. The magnitude of the inrush current is approximately the same and thus the depth of the voltage drop is approximately the same.

Figures 1.5 and 1.6 represent tests performed during a previous EPRI project that demonstrate the inrush current and subsequent voltage drop of several torque assist devices currently on the market. The torque assist devices clearly shorten the starting event by a significant amount, but they do not eliminate the problem.

Figure 1.5. Inrush Current of a PSC Compressor with Various Torque Assist Devices Installed. [2]

Figure 1.6. RMS Voltage Drop caused by Inrush Current of a PSC Compressor with Various Torque Assist Devices Installed. [2]

While the use of a torque assist device can greatly reduce the time required for the compressor to start, it can cause several adverse effects for a device attempting to actually correct the voltage drop. Since the capacitors typically used in a torque assist device are non-polarized electrolytic capacitors, they tend to not have the same amount of capacitance in both directions of voltage change. When connected to a PSC SPIM's auxiliary winding, the non-uniform capacitance can cause the inrush current to have a slight DC component, and the inrush current is not completely symmetrical with respect to the positive and negative RMS currents. This in turn causes an unsymmetrical voltage drop with respect to positive and negative RMS voltages. This unsymmetrical voltage drop is normally insignificant, but can become quite an issue if the torque assist device's capacitance is substantially larger than what is required.

Another side effect of a torque assist device on possible voltage drop correction is that when the capacitance is removed from the circuit, the current drawn by the compressor dramatically decreases instead of smoothly transitioning to steady state current. The quick removal of torque from the motor can also cause the current to become unstable, with a phase angle that can vary radically throughout several cycles.

Shunt Capacitance Flicker Suppression

Shunt capacitance is used widely throughout the power system for power factor correction, VAR support, and voltage correction. To correct the voltage flicker problem, capacitance can be connected in parallel (shunt) with the compressor to provide on demand voltage correction. In many situations where voltage flicker is an issue, all that may be needed is simple power factor correction, where the reactive power of the shunt capacitor can deliver the reactive power required by the starting event of the induction motor. This effectively lowers the inrush current and consequent voltage drop.

However, the use of shunt capacitance also allows for over correction of the power factor if the inrush event still causes significant voltage flicker at unity power factor. By operating at a leading power factor, the leading current drawn by the capacitor will cause a voltage rise across the inductive elements in series with it (i.e., distribution transformers and transformer secondary conductors.)

Figure 1.7 is a phasor diagram to demonstrate the locus of the compensated voltage for measurements made on a 4-ton unit that is known to cause perceivable voltage flicker. The phasor diagram shows the initial system voltage and the measured starting voltage, as well as voltage phasors corresponding to the calculated shunt capacitance required to correct the voltage to the compensation levels of 2% and 0% voltage drop. As expected, the addition of capacitance creates an increasingly leading phase shift of the corrected voltage.

Figure 1.7. The Phasor Diagram of the Calculated Capacitance Required to Meet a Correction Factor of 2% and for Full Correction.

To better understand how much shunt capacitance would be required for various installations, the compressors outlined in [1] as well as the several measured compressors were matched against the previously stated low, average, and high impedances. The capacitance required to meet a 2% and full compensation level was calculated along with the resulting phase shift. Table 1.2 outlines each compressor's characteristic used in the calculations. Tables 1.3, 1.4, and 1.5 depict the results of calculations on the compressors supplied in [1] to meet the compensation levels for the low, average, and high impedances in [2], respectively.

Compressor names are tagged first by the type, piston or scroll, followed by the number of that type of compressor. A letter after the number designates the test number and a 'c' designates that a torque assist device had been installed for that test. For

example, ‘Scroll4b/c’ was the second test on the fourth scroll compressor examined and a torque assist device was installed for that test.

Table 1.2. Compressor characteristics
used in the calculations to determine the required amount
of shunt capacitance needed for specific levels of voltage correction. [1]

Compressor	Vstart (V)	Istart (A)	PF	Rm (Ohms)	Xm (Ohms)
Scroll 4-Ton	223.50	132.25	0.74	1.259	1.128
Piston1a	245	75.3	0.77	2.505	2.076
Piston1b	236.1	74.4	0.78	2.475	1.986
Piston2	240.1	81.96	0.77	2.256	1.869
Piston3	239.7	60.85	0.73	2.876	2.692
Scroll1	246.9	94.7	0.75	1.955	1.724
Scroll2	222.6	135	0.76	1.253	1.072
Scroll3a	236	134.1	0.77	1.355	1.123
Scroll3b	231	139.3	0.75	1.244	1.097
Scroll3c/c	225	178	0.87	1.100	0.623
Scroll4	228.9	129.6	0.75	1.325	1.168
Scroll5a	225	141	0.61	0.973	1.264
Scroll5b	221.8	133.3	0.86	1.431	0.849
Scroll6a	224.2	188.2	0.82	0.977	0.682
Scroll6b/c	220.8	185.6	0.90	1.071	0.519
Scroll6c/c	221.9	196.6	1.00	1.129	0.000
Scroll6d/c	223.1	195.2	1.00	1.143	0.000

Table 1.3. Low Impedance capacitance values.

Compressor	Voltage Drop (%)	Full Correction Capacitor (uF)	Phase Shift (deg)	2% Correction Capacitor (uF)	Phase Shift (deg)
Scroll 4-Ton	2.29	1647	-1.2	212	-0.60
Piston1a	1.18	839	-0.65	-	-
Piston1b	1.20	854	-0.67	-	-
Piston2	1.31	932	-0.72	-	-
Piston3	1.00	709	-0.51	-	-
Scroll1	1.49	1061	-0.79	-	-
Scroll2	2.32	1674	-1.26	237	-0.66
Scroll3a	2.17	1557	-1.20	121	-0.60
Scroll3b	2.32	1674	-1.24	238	-0.64
Scroll3c/c	2.73	1985	-1.89	540	-1.27
Scroll4	2.19	1571	-1.16	136	-0.56
Scroll5a	2.55	1836	-1.05	402	-0.45
Scroll5b	2.11	1520	-1.42	82	-0.81
Scroll6a	3.05	2225	-1.89	781	-1.27
Scroll6b/c	2.77	2021	-2.08	574	-1.45
Scroll6c/c	1.71	1239	-2.44	-	-
Scroll6d/c	1.69	1222	-2.41	-	-

Table 1.4. Average Impedance capacitance values.

Compressor	Voltage Drop (%)	Full Correction Capacitor (uF)	Phase Shift (deg)	2% Correction Capacitor (uF)	Phase Shift (deg)
Scroll 4-Ton	3.60	3129	-3.31	1373	-1.20
Piston1a	1.91	1603	-1.73	NA	
Piston1b	1.96	1649	-1.80	NA	
Piston2	2.12	1785	-1.93	99	0.07
Piston3	1.57	1301	-1.35	NA	
Scroll1	2.36	2000	-2.12	304	-0.10
Scroll2	3.70	3230	-3.47	1465	-1.34
Scroll3a	3.48	3028	-3.28	1273	-1.17
Scroll3b	3.67	3199	-3.40	1437	-1.28
Scroll3c/c	4.83	4426	-5.34	2553	-3.04
Scroll4	3.45	2995	-3.18	1245	-1.08
Scroll5a	3.62	3106	-2.85	1374	-0.77
Scroll5b	3.71	3286	-3.92	1496	-1.75
Scroll6a	5.10	4666	-5.34	2793	-3.04
Scroll6b/c	5.10	4746	-5.92	2835	-3.57
Scroll6c/c	4.68	4528	-7.07	2541	-4.61
Scroll6d/c	4.63	4462	-6.97	2482	-4.52

Table 1.5. High Impedance capacitance values.

Compressor	Voltage Drop (%)	Full Correction Capacitor (uF)	Phase Shift (deg)	2% Correction Capacitor (uF)	Phase Shift (deg)
Scroll 4-Ton	8.78	3033	-8.17	2319	-5.94
Piston1a	4.78	1506	-4.14	872	-2.24
Piston1b	4.90	1550	-4.31	913	-2.40
Piston2	5.28	1683	-4.63	1040	-2.69
Piston3	3.95	1218	-3.20	600	-1.37
Scroll1	5.88	1893	-5.10	1242	-3.13
Scroll2	9.00	3141	-8.60	2416	-6.34
Scroll3a	8.49	2931	-8.10	2218	-5.88
Scroll3b	8.94	3106	-8.41	2386	-6.17
Scroll3c/c	11.45	4532	-14.01	3651	-11.14
Scroll4	8.44	2894	-7.83	2187	-5.64
Scroll5a	8.95	2999	-6.96	2311	-4.84
Scroll5b	8.95	3222	-9.82	2467	-7.44
Scroll6a	12.10	4773	-14.01	3891	-11.14
Scroll6b/c	12.00	4978	-15.92	4023	-12.78
Scroll6c/c	10.92	5166	-20.20	3992	-16.25
Scroll6d/c	10.80	5053	-19.79	3905	-15.93

From the tables of calculated capacitance, it is clear that the worst case scenario for each compressor is the high impedance, as expected. The worst case overall is the ‘Scroll6c/c’, which operates at unity power factor and requires over 5100 μF in order to achieve full compensation. This worst case is an acceptable amount of capacitance when evaluating the capacitor options available for a shunt capacitance compensation device.

The capacitor technology of choice for such a device is definitely non-polarized electrolytic capacitors because they are very cost effective per joule and are physically smaller per joule than their non electrolytic counterparts. This style of capacitor is commonly used in motor starting applications and is typically the type of capacitor supplied with any torque assist device. The only drawback to non-polarized electrolytic capacitors is that they must be used in situations that have a relatively large duty cycle;

else the buildup of hydrogen and other off gases can lead to failure. The large duty cycle should not be an issue for the application of electrolytic capacitors to voltage compensation since there is already a fairly low duty cycle associated with residential heat pumps.

Voltage Flicker Standards

There are currently two commonly used standards that address voltage flicker. Neither of which addresses the length of a voltage drop during a single inrush event. Both the Modified GE Flicker Curve, published in IEEE Standard 141,[3], and the IEC/IEEE 1453, [4], standard were developed with continuous cyclical loading in mind and fall short of completely explaining the human perception of single inrush events.

The original GE Flicker Curve was developed in the 1920s to evaluate the human response to lower-frequency flicker oscillations created by low-speed, motor-driven, reciprocating compressors. The curve was later modified to include visibility and irritability curves for voltage drop versus the frequency of the flicker events. The Modified GE Flicker Curve, Figure 1.8, fails to include the length in time of the voltage drop per flicker event. For example, according to the curve, a half-cycle flicker event is indistinguishable from a 30 cycle flicker event with respect to the allowable depth in voltage drop.

Figure 1.8 The Modified GE Flicker Curve Published in IEEE Standard 141[4].

IEC/IEEE 1453 was originally created to determine the irritation and visibility levels of arc furnace induced flicker on the utility distribution level through the use of a flicker meter. This flicker meter is designed to determine the irritability level of continuous voltage flicker, and does not address a single event in time. What the IEC/IEEE 1453 standard does show is that there is a significant distinction between rectangular and sinusoidal modulation of voltage flicker. Table 1.6 shows the allowable normalized flicker meter response for both sinusoidal and rectangular modulation. This distinction is particularly interesting when applied to the signature of voltage flicker produced by a compressor motor since elements of both the rectangular and sinusoidal modulation are present. Figure 1.9 shows an inrush event for a scroll 4-Ton compressor, including the inrush current and subsequent voltage drop with an envelope drawn around the voltage drop to show both characteristics.

Table 1.6 IEC/IEEE 1453
Normalized Voltage Fluctuation for Sinusoidal and Rectangular Modulation

Normalized flicker meter response for <i>sinusoidal</i> voltage fluctuations				Normalized flicker meter response for <i>rectangular</i> voltage fluctuations			
Hz	Voltage fluctuation %	Hz	Voltage fluctuation %	Hz	Voltage fluctuation %	Hz	Voltage fluctuation %
0.5	2.457	10.0	0.339	0.5	0.600	10.0	0.264
1.0	1.463	10.5	0.355	1.0	0.547	10.5	0.280
1.5	1.124	11.0	0.374	1.5	0.504	11.0	0.297
2.0	0.940	11.5	0.394	2.0	0.471	11.5	0.309
2.5	0.814	12.0	0.420	2.5	0.439	12.0	0.323
3.0	0.716	13.0	0.470	3.0	0.421	13.0	0.369
3.5	0.636	14.0	0.530	3.5	0.407	14.0	0.411
4.0	0.569	15.0	0.593	4.0	0.394	15.0	0.459
4.5	0.514	16.0	0.662	4.5	0.371	16.0	0.513
5.0	0.465	17.0	0.737	5.0	0.349	17.0	0.580
5.5	0.426	18.0	0.815	5.5	0.323	18.0	0.632
6.0	0.393	19.0	0.897	6.0	0.302	19.0	0.692
6.5	0.366	20.0	0.981	6.5	0.282	20.0	0.752
7.0	0.346	21.0	1.071	7.0	0.269	21.0	0.818
7.5	0.332	22.0	1.164	7.5	0.258	22.0	0.853
8.0	0.323	23.0	1.262	8.0	0.255	23.0	0.946
8.8	0.321	24.0	1.365	8.8	0.253	24.0	1.072
9.5	0.330	25.0	1.472	9.5	0.257	40.0	3.460

Figure 1.9 A Scroll 4-Ton Compressor Inrush Capture with a Voltage Flicker Envelope Around the Actual Voltage Drop of 7.6%.

The voltage flicker caused by compressor motor inrush is initially rectangular as the compressor draws locked rotor current, but as the motor accelerates to full speed, the voltage recovers in an almost sinusoidal fashion. The fact that neither flicker standard adequately describes the voltage flicker from a starting compressor motor led to the development of a laboratory experiment in human factors threshold testing to determine the actual threshold of perception. The actual threshold of perception can be used to determine the amount of compensation required by the shunt capacitance.

Summary

This chapter reviewed the basic concepts of residential heat pumps and compressor characteristics. A brief description of issues in the residential power service was given to demonstrate possible areas where voltage drop may occur during the starting of a compressor. The present standards for voltage flicker were discussed and the conclusion was reached that a flicker study should be conducted to find the actual visible level of voltage flicker such that it can be fully compensated. A description of the current technology used to alleviate voltage flicker was presented, along with the proposed use of shunt capacitance to actually compensate for the voltage flicker at its root cause. The next chapter will outline the design, test procedure, and results of the human factors flicker study to find the threshold of voltage flicker visibility.

CHAPTER TWO

HUMAN FACTORS FLICKER TESTING

After reviewing both standards used to describe voltage flicker in the previous chapter, it is clear that neither the Modified GE Flicker Curve nor the IEC/IEEE 1453 correctly address the visibility of voltage flicker created by a starting compressor motor. This chapter will discuss how a human factors study was performed to determine the actual threshold of perception for typical voltage flicker events caused by compressor motor inrush current signatures. The study was conducted in a manner commonly found in the field of psychophysics, which routinely uses methods of detection theory to find the thresholds of specific stimuli.

A two-alternative forced choice (2AFC) procedure was used with an up-down staircase method to increase the efficiency of testing while discouraging bias. The 2AFC procedure lends itself to use with an adaptive procedure, such as a staircase method, because it has a much lower bias when compared to a simple “yes-no” test. The use of a staircase method allows for greater testing efficiency by adjusting the stimulus level according to previous responses and quickly narrowing down on the threshold of perception.

Two-Alternative Forced Choice Staircase Method

A two-alternative forced choice procedure presents a subject with two intervals of different levels of stimuli and requires them to choose which interval contained the tested stimuli [5]. These intervals are typically signified by an auditory trigger when testing for visual stimuli. For the purposes of the voltage flicker study, one interval contains the voltage flicker event, while the other contains no voltage flicker. The interval that contains the voltage flicker event is chosen at random for each forced choice and the subject is required to then choose which interval they saw the flicker in. An auditory trigger was implemented in the study as a succession of beeps that signified the start and end of each interval.

A 2AFC procedure greatly reduces the subject bias by forcing them to choose which interval contained the stimulus. In a simple “yes-no” procedure, a subject can be biased with their answer if they are uncertain if the stimulus was present, whereas the 2AFC forces the subject to guess and helps to ensure a probability of near 50%. A 2AFC procedure does not completely guarantee a probability of 50% as a subject might be prone to choosing a specific interval in the case of uncertainty [5].

The staircase method attempts to converge on the threshold by adapting the stimulus level to the subject’s correct or incorrect answers. The specific staircase method used is a two-up/one-down method that requires the subject to answer correctly twice in a row before moving up one step and the stimulus level is decreased. If the subject answers incorrectly at any point the stimulus level will increase, effectively moving down

to the previous step. In the voltage flicker study, the stimulus is the voltage drop with the assumption that a larger voltage drop is more visible.

For each step up the voltage drop is attenuated according to the present voltage drop with respect to the nominal voltage. The staircase method utilizes the change in direction of the stimulus level movement, termed reverses, to allow for change in the attenuation of the step size. The attenuation allows for the staircase method to quickly converge an envelope around the experimental threshold. At first, the attenuation is coarse to allow for faster convergence, and is then reduced to a finer value after the second reverse to allow for a tighter envelope around the experimental threshold. Figure 2.1 demonstrates the attenuation verses the number of reversals in the staircase method.

Figure 2.1 An Example Graph of the Staircase Method Using a Two-Up/One-Down Response

The staircase method performed with a two-up/one-down response sequence provides the probability of 70.7% that the actual threshold lies at or above the average reverse value. The voltage flicker study allows for six total reversals, where the voltage drop values of the last four reversals are averaged to determine the experimental threshold. This experimental threshold can then be used as the threshold of perception for determining the compensation requirements of the voltage flicker suppression device.

The Test Setup and Procedure

A Visual Basic program was created to allow the testers to easily operate the equipment and perform the tests. The source code, along with screen shots, of the Visual Basic program can be found in Appendix A. An ELGAR SmartWave 5250 A was used as the waveform generator and allows the program to directly interface with it through a GPIB port. The ELGAR's resolution was confirmed with an oscilloscope to be reasonably accurate for step sizes within a $0.05 V_{\text{rms}}$ of the nominal voltage, $120 V_{\text{rms}}$.

Both the computer and the ELGAR were placed in a dark room with a single 100 W incandescent light bulb. A single point source of light was deemed to be the situation that would produce the most visible flicker. The initial voltage drop was set to 2% of nominal voltage, with an initial step size of 10% and a final step size of 3%. These values were set by experimental means to allow for the most efficient testing while not sacrificing threshold envelope size.

Since it was outlined in IEC/IEEE 1453 that there is a significant difference between a step change in voltage verses a smooth transition in voltage, both a step sequence and ramp sequence were programmed and tested. The step sequence consisted of a sharp voltage drop and recovery lasting the length of the sequence in cycles. The ramp sequence also had a sharp initial voltage drop but used a smoother three cycle recovery for a combined sequence length in cycles. To ensure consistency between forced-choice intervals, the interval with the stimulus ran the corresponding sequence with a voltage drop set, while the interval without the stimulus ran the same sequence with no voltage drop set.

It was determined that for the sake of time and participants interest level, only four tests at sequence lengths of 5 and 10 cycles would be required for both the ramp and step sequence. This allows for a fair amount of confidence in the mean threshold when averaging four tests per participant for each sequence and length.

Participants were also able to view the present voltage level of the flicker event. This was permitted because all four participants were familiar with the voltage flicker problem and it allowed for an open discussion with the participants on the level of visibility for specific voltage ranges and thus some sense of irritability of the actual voltage flicker event.

Before testing could begin, the test procedure and selection of human subjects was approved by the Internal Review Board of Clemson University to ensure the protection of all subjects and that no ethical issues might arise from the study.

Flicker Testing Results

The average value of the four threshold tests for each participant has been calculated for all four variations in voltage drop. These results are presented in Figure 2.2 as a bar graph versus the percentage of remaining voltage. During all of the tests, the nominal voltage was 120 V with a 100 W incandescent light bulb used as the single source point of light.

Figure 2.2. The Flicker Study Results showing the Calculated Thresholds for all Four Participants on all Four Test Cases

From the calculated thresholds it can be seen that there is very little variation between the four different types of voltage drop. There is relatively no difference between 10 cycles and 5 cycles for either the step or ramp sequence, and both the step

and ramp appear to give the same threshold levels. The tests clearly indicate that less than 1% of voltage flicker is visible by the human eye, but these calculated results can be slightly misleading as to the actual needs of voltage flicker compensation.

Because each participant was allowed to view the value of remaining voltage during the testing process, they were able to give feedback as to how they were able to distinguish which interval had the voltage flicker event and give their overall opinion in terms of annoyance. This feedback gave a slightly different picture than the calculated threshold results.

All participants agreed that as the voltage drop was decreased to around 1%, they were no longer actually seeing the flicker, but were relying on the fact that they could physically feel their eye adjust instead of seeing the flicker. The phenomena was described as, “the feeling your eyes have when they are trying to quickly refocus.” When asked their opinion on whether they thought they would be able see this flicker if they were not so attentive and aware that it was going to happen, the unanimous decision was that they would not.

This leads to the conclusion, that if a voltage correction device were able to compensate for the voltage drop within a 1% margin of the nominal voltage, it would definitely be within the perceived and possibly calculated threshold of non-visible voltage flicker.

Summary

This chapter discussed the design, procedure, and results of the human factors flicker study conducted to find the experimental threshold of voltage flicker. It was deemed that a compensation margin of 1% within nominal voltage should be sufficient to ensure a minimal amount of voltage flicker.

The next chapter is used as an introduction to the voltage flicker suppression device (VFS) and discusses several aspects that make the technology able to meet the compensation margin of 1% voltage drop.

CHAPTER THREE

VOLTAGE FLICKER SUPPRESSION DEVICE TECHNOLOGY

This chapter will discuss different design requirements of the Voltage Flicker Suppression Device (VFS) as they apply to the device's electrical location and voltage compensation abilities. The electrical location of the device plays a large role in the required compensation of the VFS as the impedance of branch circuit conductors can introduce a voltage drop between the VFS and the breaker panel. Since the breaker panel is the common point for an entire residence, this is the point at which the desired compensation level is required.

The initial VFS design was to create a device that can correct the voltage flicker within a 1% compensation margin at the location of the VFS. However, due to the dynamics of a residential power service, the actual desired level of the 1% compensation margin with respect to nominal voltage can change based on the branch circuit impedance between the breaker panel and the VFS installed location. This issue is addressed in this chapter and the implemented solution for finding an acceptable level for the compensation margin is presented.

Electrical Location Considerations

The design goal of the VFS is to provide voltage flicker compensation in a non-intrusive, one-size-fits-all package able to be easily and cost effectively retrofitted to

various types of residential heat pumps, be they split systems or package units. To be a non-intrusive device, the VFS must be installed such that it does not interfere nor tamper with the existing heat pump installation in terms of thermostat or motor contactor control.

The electrical location of the VFS has been chosen to provide easy installation while not sacrificing reliability in terms of detecting the compressor starting event. There is, however, a practical limitation to this installation with respect to the amount of desired compensation. This is further discussed in the next section of this chapter.

Since the VFS cannot tamper with the existing heat pump controls, the desired electrical location is for the VFS is to be spliced in parallel with the compressor such that it will be fed from the same breaker and conductors as the compressor. This circuit typically already has the ampacity to handle the possible increased current load of the VFS.

Figure 3.1 The Electrical Location Diagram of the VFS.

More specifically, the VFS is to be connected between the NEC® mandated exterior pull disconnect and the condensing unit or package unit, with supplied conductors for the compressor running through the VFS enclosure. This will allow the

VFS the ability to measure voltage at the compressor and current to the compressor, both of which are essential to any control scheme. Figure 3.1 shows the electrical location diagram of the VFS, and the actual connection diagram per NEC® regulations is located in Appendix B.

Required Voltage Compensation Level

The results of the flicker study have shown that a rather tight, 1% margin of voltage compensation is required to meet the design goal of eliminating flicker visibility. While the 1% margin of compensation can be met by the VFS at its terminals, this may not address the actual panel voltage given the chosen electrical location of the device. If the VFS was located physically close to the breaker panel, the VFS could simply operate with a compensation level of nominal voltage. However, if the conductors of the branch circuit between the breaker panel and the VFS are appreciably long or are undersized, a significant voltage drop is produced on the branch circuit. Because the branch circuit is largely resistive, little to no voltage rise created by the VFS will be seen across it.

To illustrate the problem, the following example is given. A compressor is installed 50 feet away from the breaker panel and is connected with #6 AWG, at a resistance of 0.49 Ω per 1000 feet and negligible reactance. The VFS is installed at the compressor and the total resistance between the VFS and the breaker panel is 0.049 Ω . The VFS's compensation level is set to nominal voltage, and thus the voltage at the VFS will be compensated between 99% and 100% of nominal. If the VFS and compressor

combined draw a current of $130\text{ A}_{\text{rms}}$, the equivalent voltage drop between the VFS and the panel is now $6.37\text{ V}_{\text{rms}}$. Thus the voltage seen at the breaker panel during the compressor start is the compensated voltage plus $6.37\text{ V}_{\text{rms}}$. This represents a 2.6% voltage rise at the panel if the nominal voltage is $240\text{ V}_{\text{rms}}$. This is not acceptable given the desired compensation margin of the flicker study. Instead, the desired compensation level of the VFS should be 97.4% of nominal voltage given 1% margin of compensation between 96.4% and 97.4% of nominal voltage.

There are several ways to address this issue of over-correction at the panel. The VFS location could be moved physically close to the panel, such that the voltage drop between the two is negligible. This option may not be feasible due to limited wall space near the panel or expense of installation.

The second way to mitigate the problem is to power the VFS control from another branch circuit that will not be carrying the inrush current of both the VFS and compressor. It is not required that the VFS control be powered by the branch circuit that connects to the compressor, it only needs to be able to measure current to the compressor. If a separate, dedicated branch circuit was used, the VFS control could effectively measure the actual panel voltage and compensate accordingly. Again, this option may not be feasible due to the accessibility of wiring separate branch circuits into the panel or costly installation.

The third possible solution may not be as exact as the previous two solutions in terms of knowing the correct compensation level, but offers a very cost effective answer to the problem by attempting to correct for it programmatically. It is anticipated that a

relatively reasonable estimate of the compensated voltage drop between the panel and the VFS can be easily made by the microcontroller if the initial voltage drop on the branch circuit is measured. It would only require two simple measurements and a calculation to be made with a volt meter prior to installation.

The method of calculating the initial inrush current voltage drop across the branch circuit due to only the compressor starting is as follows. With the compressor on, measure both the voltage at the panel and the compressor to get the voltage drop across the branch circuit during steady stage conditions. This voltage drop can then be used to calculate the inrush current voltage drop due to the compressor alone by scaling it by the ratio of the locked-rotor current divided by the full load current. The resulting value is effectively the expected voltage drop during the compressor starting event. Equation 3.1 demonstrates this calculation, where I_{LRA} is the locked-rotor current and I_{FLA} is the nominal steady stage current. Both of these values are available on the nameplate of the heat pump.

$$V_{BranchDrop} = \left(1 - \frac{V_{compressor}}{V_{panel}}\right) \left(\frac{I_{LRA}}{I_{FLA}}\right) \quad (\% \text{ Voltage Drop}) \quad (3.1)$$

The value of the initial inrush voltage drop can easily be set on the microcontroller by using a series of dip switches that correspond to predetermined increments of voltage. An example worksheet to be used by the installing technician can be found in Appendix B.

The estimated voltage drop at the panel can then be used by the microcontroller to perform correction within 1% of the estimated value. Even with the panel voltage estimate, it is possible to implement either of the other two solutions by simply forcing the $V_{\text{BranchDrop}}$ to be zero, and thus Equation 3.2 will simply yield the measured voltage drop.

Adaptive Capacitance Technology

To retrofit the VFS to any existing compressor installations without prior knowledge of the distribution system impedance at the install location, a one-size-fits-all design has been adopted. Since the capacitance required to achieve the compensation requirements can vary greatly from hour to hour during high demand, and month to month in certain regions of the US where non-electric heat is common, it is essential that the VFS be able to vary its capacitance to meet the ever changing system requirements.

A capacitor scheme has been created through the use of staged capacitance to allow the VFS to adapt to the capacitance required for almost any combination of compressor and distribution system characteristics. The capacitors in which the scheme has been designed around are non-polarized motor start electrolytic capacitors. As stated before, these capacitors offer a cost effective solution for large capacity, short duration applications. There are two different types of motor start capacitors used on the VFS. The first type was specially designed and manufactured by Cornell Dubilier for this project, and consists of 900 μF non-polarized electrolytic capacitors rated at 450 V_{ac} .

The second type is off the shelf motor start non-polarized electrolytic capacitors, where 300 μF is the largest available size for a 240 V_{ac} application.

These capacitors are arranged into four full stages and two tuning stages that allow for the VFS to adjust the capacitance in increments of 300 μF . A full stage, each consists of a single 900 μF specially designed capacitor. The first tuning stage, 1/3 of a stage, is a single 300 μF capacitor and the second tuning stage, 2/3 of a stage, is comprised of two 300 μF capacitors for a total capacitance of 600 μF . Table 3.1 demonstrates the layout of the capacitors in stages, as well as the designated stage number and IO address used by the controller for each stage.

Table 3.1 Staged Capacitance Outline

Stage Number	Stages	Capacitance (μF)	I/O Address
0	0	0	000000
1	1/3	300	100000
2	2/3	600	010000
3	1	900	001000
4	1 1/3	1200	101000
5	1 2/3	1500	011000
6	2	1800	001100
7	2 1/3	2100	101100
8	2 2/3	2400	011100
9	3	2700	001110
10	3 1/3	3000	101110
11	3 2/3	3300	011110
12	4	3600	001111
13	4 1/3	3900	101111
14	4 2/3	4200	011111
15	5	4500	111111

The selection of increments in values of 300 μF is not completely by the sizing limitations of the motor start capacitors. It can be directly derived from the shunt capacitance calculations for the various types of compressors when taking into account the compensation requirements. The least amount of shunt capacitance required to move

a compressor from 2% correction to full correction is 600 μF . This means that the use of staging in increments of 300 μF should give the VFS the ability to compensate within a 1% margin of voltage compensation.

Summary

This chapter discussed the importance of the electrical location with respect to voltage compensation and possible methodologies to ensure the correct level of compensation at the breaker panel within a residence. An overview of the capacitance layout that allows for the VFS to compensate at almost any installation by adapting its seemingly variable capacitance is also given in this chapter.

The next chapter will outline the basic design of the VFS along with specifics about hardware components and limitations that these components might introduce on the compensation abilities of the VFS.

CHAPTER FOUR

VOLTAGE FLICKER SUPPRESSION DEVICE HARDWARE

The development of the voltage flicker suppression device (VFS) has been based on three basic design principles: simplicity, reliability, and flexibility. These principles have been applied to the electrical location of the device as well as the hardware layout, components, switch design, and control algorithms.

The basic outline of the VFS consists of capacitors used for compensation, current and voltage measurement circuits for control, semiconductor switches to perform the insertion and removal of the capacitors, a DC power supply used to power the controller, and the microcontroller itself. All of these items combine to allow the VFS to detect the compressor starting event, insert the correct amount of capacitance for the desired compensation, and remove the capacitance as the compressor accelerates such that the voltage flicker is minimized.

The complete circuit schematic is shown in Figure 4.1. The schematic shows all essential components to the design as well as terminal labeling used for capacitor stage identification and connection. A bill of materials (BOM), along with the pictures of the final lab prototype can be found in Appendix C.

Figure 4.1. The VFS PC Board Circuit Schematic.

Hardware Considerations

There are several items that are ancillary with respect to the main hardware components, including: the step-down transformer, printed circuit board, over current and over voltage protection, and isolation requirements between the high voltage and control circuits.

A low power, four winding control transformer is used to step-down the line voltage to a manageable level for both the DC power supply and voltage measurement. The transformer consists of two high voltage windings that are connected in series to yield a rated voltage of $240 V_{ac}$. The secondary windings, rated at $16 V_{ac}$ each, are operated and rectified independently; one for the DC power supply and the other for use as a potential transformer.

The printed circuit board (PCB) requires special consideration since the full load current of each capacitor stage will be flowing through different traces on the board. The PCB is designed with two layers and a thickness of 0.062". The heaviest weight of copper available, 2.5 oz/ft², and trace thicknesses of 0.2" are used for all current carrying traces on the board. These traces are limited to less than ¼ " in length. The actual capacitor connections to the PCB are through crimp-on ring terminals that mate with screw terminals soldered directly to the PCB. The PCB also houses the over current protection for each capacitor stage as well as for the control circuit, with fuse holders soldered directly to the PCB.

The over current protection for the VFS capacitor stages is provided using Ferrez-Shawmut TRM slow-blow fuses rated at 30 A for the full stages and 15 A for the two tuning stages. The fuses chosen are designed for high inrush currents and have a long clearing time given their operation within the VFS. For example, a full stage of capacitance can draw nearly 90 A through the 30 A fuse, but the clearing time for the fuse at this current level is 3 seconds. The fuses also have an acceptable interruption rating of 10 kA. Another 5mm by 20mm slow-blow fuse is used to protect the control transformer.

Over voltage and surge protection for the PCB is provided by the use of three metal oxide varistors (MOVs). These devices are not intended to protect against momentary over voltages but more to protect against surges possibly caused by lightning. The protection against momentary over voltages is designed into the DC power supply and voltage measurement circuit by either the over rating of components or by other means.

It is essential to have a fair degree of isolation between the power and control circuits to prevent potentially damaging break over currents. All components that interface between the high power and low power circuits are rated for a minimum of 1500 V_{ac} isolation. This will help protect the control circuitry in the situation where an MOV might have sufficient transient voltage suppression capabilities.

Isolated TRIAC Switch Design

The switch design is built off of a commonly found circuit that uses an optically isolated pilot TRIAC to drive a larger TRIAC. This circuit is used to drive high power devices from low power control circuits while keeping a high degree of isolation between the two. A Teccor Q4040K7 is used as the high power TRIAC device and is rated for a continuous current of 40 A at a rated operating voltage of 400 V_{peak}. This semiconductor device is actually an alternistor, which provides a superior static dV/dt of 1100 V/μs in comparison to typical power TRIACs.

A Fairchild FOD420 optically isolated pilot triac is used to gate the alternistor through a 380 Ω resistor to limit inrush current. The FOD420 is a new variation on the traditional opto-isolated pilot triac in that it is a snubberless design and offers a static dV/dt of 10 kV/μs. The forward bias current required for triggering of the FOD420 is also very low, 5 mA. The decision was made to use the FOD420 after several incidents proved that the static dV/dt of the previously used device was insufficient and would require a snubber circuit. Without a snubber circuit, the main power TRIAC was allowed to enter avalanche breakdown if power was applied to the VFS when the line voltage was near a peak.

It should be noted that since the switch design is built around a TRIAC device, the switch will only turn off at a zero crossing of the current. Since they are switching capacitors in and out, the switch will not turn off until the voltage reaches a peak. This will prove to be a limitation for controller design by introducing a time delay.

Voltage and Current Measurement Circuitry

The voltage measurement is performed by using one of the secondary windings of the step-down transformer as a potential transformer (PT). In order to condition the voltage signal for the microcontroller's analog-to-digital converter (ADC), the voltage must be rectified and reduced via a resistive divider. Schottky diodes are used for the full-wave rectifier because of their low forward voltage drop. Since the voltage measurement will also be used for a zero-cross detector, the low forward voltage drop is required. The negative side of the rectified DC bus is connected to the controller reference for use with the ADC.

The resistive divider consists of a 5.6 k Ω resistor acting as the voltage drop with the measurement being taken across a 3.3 k Ω resistor. The effective peak voltage measurement from the resistive divider is 4.2 V_{peak} for a given transformer primary voltage of 240 V_{ac} nominal. In anti-parallel with the 3.3 k Ω measurement resistor is a 5.1 V Zener diode that acts as a voltage clamp in the case of a momentary over voltage to protect the ADC of the microcontroller.

Unlike the voltage measurement circuit, the current measurement circuit is separate from the PCB, and is connected to the PCB using a small jumper wire. It was chosen to leave the current transformer (CT) circuit separate from the PCB in order to allow for flexibility in VFS enclosure layouts. Earlier versions of the VFS prototype had used a hall-effect CT, but the decision was made to move to a classic style CT for simplicity and reliability purposes. The current measurement is performed using a CR

Magnetics CR8348-2000 CT. The CT burden resistance was chosen according to Equation 4.1 found on the data sheet for the device.

$$V = \frac{I * R}{Te} \quad (4.1)$$

The T_e constant for this specific CT is 2046. Given a maximum desired voltage of 5 V_{peak} , the resistance was chosen to be 40 Ω . This yields a primary current of 180 A_{rms} , which is well above the inrush current of most compressors.

Just like PT circuit, the CT circuit uses Schottky diodes arranged in a full-wave rectifier to condition the measurement signal for the ADC. The 40 Ω resistor is placed across the rectified DC bus and a 5.1 V Zener diode is placed in anti-parallel to protect the ADC from an over-current condition. Again, the negative side of the DC bus is connected to the controller reference for use with the ADC.

Microcontroller and DC Power Supply Circuitry

The DC power supply circuit is supplied from one of the secondary windings of the step-down transformer and rectified onto a DC bus with Schottky diodes. The Schottky diodes are not required in this application, but are used for consistency and to minimize the BOM. The rectified DC bus is connected in parallel to a 100 μF ripple capacitor to ensure that very little ripple voltage is seen on the 5 V_{dc} bus when the line voltage is as low as 90 V_{rms} . The negative side of the DC bus is tied to the same common point as the measurement circuits. An LM7805 is used to regulate the DC bus voltage to 5 V_{dc} for the microcontroller. The recommended AC filter capacitors are used on the

voltage regulator to couple any high frequency noise on the input and output to the common node.

The microcontroller circuitry was replicated from the Microchip demonstration board, and consists of several AC filter capacitors to couple noise to the common node, along with a buffer for the ADC, an LED indicator, and reset switch. The LED indicator is used to show the present state of the microcontroller's algorithm, while the reset switch is used to clear the EEPROM of the microcontroller and force it to retune to the correct capacitance. For the setting of the compensation level, four dip switches are used to replicate the digital switch from the Microchip demonstration board, and consist of a current limiting resistor (10 k Ω), an input resistor (1 k Ω), and a fill capacitor (0.1 μ F) that is shorted by the dip switch.

The Microchip dsPIC30F3013 is able to source 25 mA per digital IO pin up to a total of 200 mA. Each optical isolator is driven directly from the digital IO pin through a 1.5 k Ω resistor for an on-state current of 3 mA, the LED indicator is driven through a 1.5 k Ω resistor for an on-state current of 2 mA, and the reset switch will draw 0.5 mA only when pressed. For the worst possible case of all six optical isolators and the indicator LED being powered at the same time, the combined current is less than 20 mA.

Summary

A basic outline of the VFS and its hardware layout is given in this chapter. The switch design was noted as having possible limiting effects on the VFS's compensation abilities.

The next chapter will explain the control of these hardware components and how the setting of the compensation level can move the 1% compensation margin such that the desired voltage compensation is seen at the breaker panel. Detailed information about the controller algorithms will highlight the complete control cycle of how the VFS is able to tune itself to the correct capacitance and avoid false triggering that can be caused by some situations.

CHAPTER FIVE

VOLTAGE FLICKER SUPPRESSION DEVICE CONTROL

Since the VFS is to be a non-intrusive device with respect to retrofitting residential heat pumps, the only reliable way to determine when the compressor is starting is by measuring the compressor current. This will inherently introduce a small time delay, one half-cycle maximum, where the inrush current to the compressor is not being compensated because the VFS must wait until the zero crossing to insert the capacitance. Because the capacitance is always discharged to zero volts, the insertion of the capacitance anywhere but a zero crossing may result in an excessive overvoltage transient, possibly damaging household electronics and the VFS.

Another limitation for the controller comes from the implemented switch design. To completely ensure capacitor removal for all types of compressors and installations, the capacitors need to be removed by detecting a voltage rise with respect to the nominal voltage before the compressor starts. As stated before, the TRIAC switch design limits when the capacitors can be removed to the peak of the voltage, zero crossing of the current. This creates a situation where the controller knows the correct time to remove the capacitor due to a measured half-cycle voltage and responds accordingly by turning off the opto-isolator pilot triac. However, the capacitor is not actually removed from the circuit until the peak of the voltage and undesired voltage rise can spill over into the next half-cycle, causing an overshoot in voltage during the removal process. An acceptable

medium has been found through testing in which premature removals and the overshoot voltages are both minimized.

Microcontroller Considerations

The controller for the VFS is implemented on a Microchip dsPIC30F3013. This device was chosen as a good balance between functionality, processor speed, instruction size, memory, program space, and support. Its 16-bit architecture matched with a 12-bit A/D converter provides the ability to fully utilize the sensor bandwidth and not sacrifice sampling speed to lengthy calculations. The program space and memory available on the device is more than adequate for the VFS controller.

As with all microcontrollers, the operational characteristics of the microcontroller are set through registries upon startup of the program, including: the clock, brown-out detection, the ADC, digital IO ports, and onboard timers. These settings will be briefly discussed here, but the microcontroller documentation [6] and the source code should be consulted for actual registry values.

The microcontroller is set to operate at a nominal frequency of 30 MHz from an internal RC oscillator. This eliminates the need for an external crystal oscillator and saves space on the PCB. The brown-out circuit is set to turn off the microcontroller if the voltage level drops below $4.7 V_{dc}$. This level was chosen to ensure the correct operation of the capacitor switches and should not be an issue unless the line voltage drops below

90 V_{rms} . The voltage should never fall below 5 V_{dc} as the input voltage to the voltage regulator should always be sufficiently higher than 5 V_{dc} .

The ADC is configured to sample the analog input channels AN4 and AN5. The CT is connected to AN5 while the PT is connected to AN4. The ADC will sample both channels, one after another, and set the ADC interrupt flag each time both samples are complete. A while loop in the controller will wait for the ADC interrupt flag to be set and then reset the flag, allowing the ADC to start sampling again. The sampling time set for the ADC is significantly faster than the control loop.

Three digital IO ports are used to effectively control all six capacitor switches and the LED indicator. The four full stages are on IO port B, pins RB6 through RB9. The tuning stages are on IO port F, pins RF4 and RF5. The staged capacitance is mapped to these ports through the use of constants in the controller that access the correct ports based on the stage number, 0 to 15. The LED indicator is on IO port D, pin RD9.

The digital IO pins, RB0 through RB3 are reserved for the compensation level adjustment gain as mentioned in the section titled Desired Compensation Margins. These IO pins are connected directly to four dip switches, powered by the DC power supply and used as digital inputs to the microcontroller.

The dsPIC30F3013 has three 16-bit onboard timers and all three are used by the controller. Timer 1 is used to flash the indicator LED during the trigger delay. Timer 2 and Timer 3 are combined to create a single 32-bit timer that is the trigger delay timer to prevent any instantaneous retriggering of the VFS and has a timeout of 30 seconds.

Controller Operation

The basic operation of the controller is as follows: ensure that the compressor is currently off, wait for the trigger to signify the compressor is started, insert the pre-determined amount of capacitance at the next zero crossing of the voltage, remove the capacitance according to the staged removal process, perform the calculations to determine the amount of capacitance required for the next trigger, wait until the delay timer is done, inhibit triggering until the compressor turns off, then restart the process. The flowchart in Figure 5.1 represents the basic operation of the controller and the source code for the microcontroller can be found in Appendix D.

The control algorithm operates in two distinct modes: online and offline. The online mode performs measurements, calculates average values each half-cycle, and switches in and out the capacitors. The online mode runs in open-loop, meaning that it will sample the ADC as fast as it can, which is currently about 260 samples per half-cycle. The online mode will stop each half-cycle, triggered by the zero crossing of the voltage, to calculate the average values of current and voltage, determine the current state of the compressor by using the control register, and change the present state of the LED indicator. The online mode keeps a running total of the present half-cycle voltage and current and then calculates the average value for the half-cycle by dividing by the number of samples during that half cycle.

Figure 5.1. Flowchart of Basic Controller Operation

Just after the controller is initialized, it will check to see if the reset switch is active. If it is, the controller will clear the initial inrush current measured and the previously inserted amount of capacitance from the EEPROM, and thus begin retuning itself at the next compressor start by inserting zero capacitance and measuring the initial inrush current again. If the reset switch is inactive, then the microcontroller will load the previous amount of capacitance and initial inrush current from the EEPROM, and begin the online mode of operation as if it was never interrupted. This feature is necessary for the VFS to be able to offer compensation for a cold load pickup of the HVAC equipment.

The online mode uses a control register to indicate specific situations for the algorithm through the use of setting flag bits. Table 5.1 shows the state of the control register in order of operation during the compressor inrush event.

Table 5.1 Descriptions of Possible Control Register Status

Control Register	Description
000	Waiting for trigger to be set by inrush current
00F	Trigger set, insert capacitance at next half-cycle
0FF	Capacitance has been inserted, compressor is on
FFF	Capacitance has been removed, start delay
0F0	Compressor is still on, inhibit triggering

The first flag bit indicates that a trigger has been set because the compressor current has risen above the trigger set point for 10 samples in a row. The trigger flag bit can only be set if all other flag bits are not set and is cleared by the trigger delay timer. Once this flag bit is set, the pre-determined amount of capacitance required will be inserted at the next zero crossing of the voltage.

The current trigger set point is for $70 A_{\text{peak}}$ to allow for the use of 10 kW of auxiliary electric heat if the VFS is installed on a package unit and the electric heat is turned on before the compressor. The set point of $70 A_{\text{peak}}$ corresponds to an ADC value of 1100 or $2.3 V_{\text{peak}}$ from the CT. The trigger is held off from being set for 10 samples to give it a certain amount of immunity to any possible noise or current spikes on the system.

The second flag bit indicates that the compressor is currently running and that a trigger has already been acknowledged by inserting the pre-determined amount of capacitance. The compressor flag bit being set will inhibit any future trigger and the controller automatically starts with this flag bit being set. The compressor flag bit is only reset after the compressor turns off to prevent the VFS from retriggering if the auxiliary electric heat turns on because the compressor alone cannot keep up with the demand on a package unit. The compressor flag bit reset value is an average half-cycle current of less than 5 A, and allows for the exterior fan to not interfere with the compressor flag bit being reset. The flag bit also inhibits the LED indicator and forces it to remain unlit until the compressor turns off.

The third flag bit signifies that the starting event is complete and is set when all of the capacitance has been removed from the circuit by the staged control removal algorithm. This flag bit ends the online mode and starts the offline mode and trigger delay timer.

The trigger delay timer is used to prevent the VFS from re-triggering and enforce a duty cycle on the VFS. The timer is set for a 30 second interval, and will flash the

indicator LED at a 50% duty cycle with a period of 4 seconds. The 30 second interval is short enough to allow the device to re-trigger correctly for a multi-stage compressor. A multi-stage compressor that is changing between stages will stop the compressor, wait for the pressure to equalize, and then restart the compressor in another stage. These units typically have a timer built into them of 1 minute between compressor starts.

Table 5.2 LED Indicator for Controller Status

LED Indicator	Control Register	Controller Status
Constantly on	000	Waiting for trigger
Flashing every 2 sec	FFF	Delay timer active
Off	0F0	Trigger inhibited

The offline mode determines the amount of compensation required for the next inrush event by examining the voltage drop of the previous inrush event using the adaptive capacitance control algorithm. The offline mode is run before the delay timer becomes active and will save the value of the previously inserted capacitance to the onboard EEPROM to ensure that the device can recover from a blackout and quickly provide compensation for a possible starting compressor.

Adaptive Capacitance Control

The adaptive capacitance control is built around the designed layout set forth by the adaptive capacitance technology. This control works with the staged capacitance to allow the controller to learn the correct amount of capacitance needed for a particular

installation point. The control algorithm works independently of the nominal voltage of the feeder circuit by simply comparing the average voltage before the compressor started to the average voltage while the compressor is started with the capacitance in the circuit.

The online mode continuously keeps an array of the past two average half-cycle voltage values up to date while the trigger is enabled. At the point in which the trigger is set to insert the capacitance, the values for the previous two half-cycle voltages are captured, and stored as the pre-start voltage. The online control then inserts the pre-determined amount of capacitance and waits for two half-cycles to pass to ensure that the capacitance has stabilized in the circuit. It then captures the next two half-cycle average voltages and stores them as the in-start voltage.

Once the starting event is complete, the offline control calculates the full-cycle average voltage for both the pre-start and in-start voltages. It then uses these voltages to calculate the apparent voltage drop at the VFS between the pre-start nominal voltage and the in-start compensated voltage. The calculation for the measured voltage drop is demonstrated by equation 5.1.

$$V_{MeasuredDrop} = 1 - \frac{\left[\frac{V_{InStart1} + V_{InStart2}}{2} \right]}{\left[\frac{V_{PreStart1} + V_{Prestart2}}{2} \right]} \quad (5.1)$$

When power is initially applied to the microcontroller, it does not offer any voltage compensation, as it needs a starting point at which to begin deciding how much capacitance is needed. The microcontroller captures the initial inrush current at this point, I_{LRA} , and retains this value to scale the voltage drop on the branch circuit according

to the new inrush current created by the VFS and the compressor combined. This allows for an estimated voltage drop at the panel to be calculated as seen in Equation 5.2.

$$V_{PanelEstimate} = V_{MeasuredDrop} - V_{BranchDrop} \left(\frac{I_{Measured}}{I_{LRArated}} \right) - V_{SwitchDrop} \quad (5.2)$$

The final estimate of the panel voltage drop includes a calculated switch drop and is then used to determine the amount of capacitance to insert. The switch voltage drop incrementally accounts for the voltage drop across the control transformer due to each switch used during a compensation period. This is a laboratory measured value and is approximately 0.03% per switch.

The adaptive control is designed for accelerated tuning by allowing two different increments in capacitance. If the voltage drop estimate is greater than 3%, the capacitance is increased from its current value by a full stage, or 900 μ F. If the value of the voltage drop is greater than 1% but less than 3%, the capacitance is increased by only a third of a stage, or 300 μ F.

The controller has a dead band between 1% and 0% voltage drop in which no change is made to the capacitance level. If for any reason the device has been over tuned or the distribution system has stiffened, and the voltage drop is now negative, a third of a stage, 300 μ F, will be removed from the current capacitance value. These regions of voltage drop and corresponding incremental capacitance change are outlined in Figure 5.2.

Figure 5.2. Outline of the Controller Regions that Correspond to Incremental Changes in the Capacitance.

After the amount of capacitance has been set, the adaptive control will pre-calculate three variables to be utilized by the online control for insertion and in the staged capacitance removal. The first variable is TotalStages, which corresponds directly to the stage number pre-mapped to the correct IO address. TotalStages is used by the online controller to know the correct capacitance to be inserted at the next trigger. The second variable is WorkingStages and is initially equal to TotalStages. The third variable is modulo 3 of TotalStages and is called TuningStages. WorkingStages and TuningStages are used to remove the capacitance in an orderly and timely manner at the end of the starting event by the staged capacitance removal process. The TotalStages along with the initial inrush current are both saved to the EEPROM such that the VFS can quickly recover from a power outage without needing to retune itself.

Staged Capacitance Removal

It was clear early-on in the VFS development that removing all of the capacitance inserted at a single point in time would create a very large instantaneous voltage drop that would defeat the purpose of the VFS. To help smooth the voltage drop due to the capacitance, the designed layout of the adaptive capacitance technology was utilized to create a staged removal process. The staged removal process is intended to mimic the natural decay in the compressor motor inrush current as it accelerates. Figure 5.3 exemplifies the affect of the natural decay of compressor current versus a removing all of the capacitance at once and the staged capacitance removal process.

As the compressor motor accelerates and the inrush current decays, the amount of capacitance that is inserted begins to cause a voltage rise. When the trigger is set to insert the capacitance, the value of the cutoff voltage is calculated as a percentage of the in-start voltage. Lab testing showed that a value of 100.7% of the in-start voltage allowed for the correct removal of capacitance while eliminating most premature removals. Once the capacitance has been inserted, the staged removal process waits until the previous half-cycle voltage is greater than the cutoff voltage and removes the desired amount of capacitance.

Figure 5.3. An Example of the Need for Staged Capacitance Removal in order to Achieve a Smoother Voltage Transition.

The staged removal process uses the variables `TuningStages` and `WorkingStages` to determine which capacitors need to be removed. The first time the half-cycle average voltage is over the cutoff voltage, the tuning stages will be removed and the `WorkingStages` variable will be set equal to the `WorkingStages` minus the `TuningStages`. If no tuning stages are present, the first full stage will be removed. For each consecutive time thereafter the half-cycle average is over the cutoff voltage, a full stage will be removed and the `WorkingStages` variable will be set equal to its current state minus three. The process continues until the `WorkingStages` variable is equal to zero and thus no stages are still in the circuit.

For the current layout of the adaptive capacitance technology, the maximum amount of cycles required for removing all four full stages and a tuning stage is 5 half-

cycles or 2.5 cycles. This works well with the compressor current inrush signature, since most compressors take three cycles to transition from locked-rotor current to steady state current. As a fail safe for the staged removal process, all capacitors are removed after 30 full cycles.

Summary

In this chapter, the specifics of the microcontroller were addressed, as well as the elements of the online and offline modes of the controller. The detailed description of the adaptive capacitance control and staged removal process demonstrate the VFS's ability to correctly adapt to the desired compensation margin as well as minimize the voltage disturbance created by removing the capacitors from the circuit.

The next chapter will review laboratory results on three different size heat pumps that represent a large cross section of the current installed-base in the US marketplace.

CHAPTER SIX

LABORATORY TESTING RESULTS

This chapter will present laboratory testing of the VFS as well as discuss the results of each test. The test results are broken down into two types of testing: the first set is to verify that the compensation margin is being met by the VFS and the second set will demonstrate the compensation level as implemented. For the purposes of testing and verifying the VFS's performance, three typical residential air conditioners were acquired. The three units provide a cross section of the equipment that could be found at VFS installations, including: auxiliary heat, package units, multistage units, and units equipped with torque assist devices.

The first unit is a Heil 2.5-Ton package unit heat pump, equipped with 10kW of auxiliary electric heat. The second unit is a 4-Ton Carrier split system air conditioner. The final unit is a 5-Ton Carrier two stage split system air conditioner that is has a factory equipped torque assist device. For each unit, eight tests were run in consecutive order to demonstrate the VFS's ability to tune itself and maintain repeatability of voltage correction for several tests.

There are two distinct design limitations that have been mentioned in previous sections that are expected in the laboratory results. The first limitation of the VFS is directly related to the fact that the device is triggered from the compressor current and must wait, at most a half-cycle, before compensation can begin. Thus it is expected to see a half-cycle of voltage drop when the compressor initially starts.

The second limitation deals with the switch design used. Since the switches used to insert and remove the capacitors are based on a TRIAC semiconductor device, it is required that the capacitor current move through a zero crossing before the device will actually turn off. Thus the VFS may remove the capacitor at the correct half-cycle voltage measurement, but the switch will not turn off until the peak of the voltage. Thus the expected results also include a slight voltage swell as the capacitors are to be removed. It was found through experimentation that a cutout voltage of 100.7% yielded the best performance in terms of minimizing both premature removals and this removal overvoltage.

A sliding window root mean square (RMS) method is used to convert the raw captured waveforms into an easily identifiable waveform, as is common with many power system waveforms. There are several issues that arise from using this method that are discussed in this chapter.

The Test Setup

The units are powered from a step-down transformer rated for 480V/240V at 37.5 kVA with an impedance of 6.5%. The high side of the transformer is connected line to line on a dedicated 480V bus rated for 500 kVA. The units and the VFS are connected to the step-down transformer through a main disconnect switch fused for 100 A and a 40 A circuit breaker. The 100 A fuses are used as backup protection in case the 40 A circuit breaker operates incorrectly. During lab testing, the 100 A disconnect was used to mimic

a false breaker panel and the 40 A circuit breaker represents the exterior pull disconnect for a typical residence. For all tests, the 40 A breaker never operated, even given the higher feeder currents created by the VFS. For comparison with the system impedances used for the initial calculation of required capacitance, Table 6.1 outlines the calculated impedances at the false breaker panel.

Table 6.1 Calculated Impedances at the False Breaker Panel

Low	Average	High
$0.0545 + i0.1003 \, \Omega$	$0.0621 + i0.0942 \, \Omega$	$0.0658 + i0.0960 \, \Omega$

For the compensation margin testing of each unit, the test runs are broken down into tuning runs followed by consecutive runs to demonstrate stability. The VFS voltage and current as well as the compressor current are measured. The feeder current is simply the point by point addition of the VFS current and the compressor current waveforms.

For the purposes of compensation level testing, 16 feet of #14 AWG Romex was used to approximately simulate 100 feet of #6 AWG branch circuit conductors between the false panel and the compensation point. The simulation of the branch circuit conductors does not adequately account for the inductance of the branch circuit, but because the X/R ratio of such conductors is rather small, 0.1, it will have a negligible effect on the results.

The compensation level testing was performed on the 2.5 Ton and 4 Ton units to gauge the panel voltage estimation scheme. Only the voltage at the VFS and the voltage at the panel are presented, as the currents are expected to be similar to those in the

compensation margin testing. Again, the results demonstrate an eight run tuning cycle, with several cycles showing the device tuned to what it believes is the correct capacitance according to the estimated panel voltage.

Figure 6.1. The Laboratory Testing Connection Diagram.

Measurements and Data Analysis

The voltage and current measurements captured during lab testing were taken using a four channel digital oscilloscope to allow for the synchronization of all measurements. For the voltage measurements, Tektronix P5200 High Voltage Differential Probes were used to isolate the oscilloscope from the measurement point. These probes allow for a maximum voltage of 1300 V_{RMS} and have a rated bandwidth of 25 MHz for 3 dB of attenuation. Current measurements were made with two AEMC

SD661 AC Current Probes, which are rated for 1000 A_{RMS} with a bandwidth of 100 kHz for 3 dB of attenuation.

These probes were connected to a Tektronix TDS 3034B digital oscilloscope rated for a bandwidth of 300 MHz with a maximum sampling frequency of 2.5 GS/s. For each test run on the VFS, the oscilloscope time scale was set for 40 ms/div, yielding a waveform capture of 400 ms long. To record the raw waveform data, the RS232 port was used on the oscilloscope, which allows for ten thousand points per waveform spaced over the waveform capture length. This yields raw waveform data that is sampled every 40 μ s, 25 kHz sampling frequency, for the entire fourth of a second capture.

To aid in the analysis of the waveform captures, a sliding window RMS calculation was performed on point by point representation of each captured waveform to yield a continuous RMS waveform. Each RMS voltage waveform was then normalized against the initial steady state value of that waveform to give an RMS waveform that is representative of the percent voltage drop as it relates to the initial steady state voltage. While this type of RMS analysis is very common within power system literature, there is a disadvantage that arises when adapting it to the analysis of the VFS's compensation ability. Figure 6.2 represents a voltage waveform capture that has been rectified for ease of comparison and the corresponding calculated RMS waveform normalized against the steady state voltage.

Figure 6.2. A Comparison of the Sliding Window RMS Waveform versus the Corresponding Rectified Waveform.

By using a full-cycle sliding window RMS calculation, voltage changes that are significant in length with respect to a single cycle will appear longer in time than the actual event. On the left hand side of Figure 6.2, a half-cycle voltage drop on the captured waveform bleeds into what appears to be a one and a half cycle long event. This is due to the fact that the half-cycle long event is observed by both the leading and trailing edges of the continuous sliding window RMS calculation. The same result can be observed for the subsequent voltage rise seen during capacitance removal. The effects of both of these events on the perceived light flicker are discussed later in this chapter.

2.5 Ton Package Unit Compensation Margin

The following graphs depict a base line run, in which no compensation was offered, followed by eight consecutive runs on the 2.5 Ton package unit. It took the unit four runs to finish tuning to the correct capacitance needed by the unit for the lab impedance. This capacitance ended up being 1200 μF . Figures 6.3, 6.4, 6.5, and 6.6 show the RMS voltage, compressor current, capacitor current, and feeder circuit current respectively. A brief discussion of the results continues after the figures.

For the first set of figures in this section, specific runs have been labeled above the corresponding waveform to clarify them for discussion purposes. The soft copy of this document should be consulted for all colored legends and waveforms.

Figure 6.3. 2.5-Ton Package Unit Voltage Measurements.

Figure 6.4. 2.5-Ton Package Unit Compressor Current Measurements.

Figure 6.5. 2.5-Ton Package Unit Capacitor Current Measurements.

Figure 6.6. 2.5-Ton Package Unit Feeder Current Measurements.

As expected, the initial half-cycle voltage drop is present as well as the removal overvoltage. This overvoltage is limited to a 2% rise for a half-cycle to one full cycle.

The compressor current graph demonstrates a side effect of the VFS that is expected when applying voltage compensation to the compressor. Since the starting torque is proportional to the square of the voltage, by compensating the voltage, the effective starting torque of the motor is increased. This can be seen as the starting time of the compressor is reduced by a couple of cycles when the voltage is compensated to within the 1% margin.

A promising result is seen in the feeder currents, which show the actual magnitude of the current drawn through the circuit breaker from the distribution system remains relatively unchanged for this unit.

4 Ton Split System Unit Compensation Margin

The following graphs depict a base line run, in which no compensation was offered, followed by eight consecutive runs on the 4 Ton split system unit. It took the unit three runs to finish tuning to the correct capacitance needed by the unit for the lab impedance. The final tuned capacitance is 2100 μF . Figures 6.7, 6.8, 6.9, and 6.10 show the RMS voltage, compressor current, capacitor current, and feeder circuit current respectively. A brief discussion of the results continues after the figures.

Figure 6.7. 4-Ton Split System Unit Voltage Measurements.

Figure 6.8. 4-Ton Split System Unit Compressor Current Measurements.

Figure 6.9. 4-Ton Split System Unit Capacitor Current Measurements.

Figure 6.10. 4-Ton Split System Unit Feeder Current Measurements.

The results of the 4-Ton unit are similar to those of the 2.5-Ton with two noticeable differences. The removal overvoltage is now a 2% rise for a definite full cycle, and the compressor starting time significantly lower for this unit when the voltage is compensated. Again, the feeder current is about the same magnitude as the compressor inrush current alone.

5 Ton Two Stage Unit Stage 1 Compensation Margin

The following graphs depict a base line run, in which no compensation was offered, followed by eight consecutive runs on the 5 Ton split system unit running in its lower capacity stage, stage 1. It took the unit 4 runs to finish tuning to the final capacitance the VFS thought was required by the unit for the lab impedance. Figures 6.11, 6.12, 6.13, and 6.14 show the RMS voltage, compressor current, capacitor current, and feeder circuit current respectively. A brief discussion of the results continues after the figures.

Figure 6.11. 5-Ton Split System Unit Running in Stage 1 Voltage Measurements.

Figure 6.12. 5-Ton Split System Unit Running in Stage 1 Compressor Current Measurements.

Figure 6.13. 5-Ton Split System Unit Running in Stage 1 Capacitor Current Measurements.

Figure 6.14. 5-Ton Split System Unit Running in Stage 1 Feeder Current Measurements.

The 5 Ton stage 1 results are very similar to the 2.5 Ton results, but with a couple of distinctive differences. Since the 5 Ton unit has a factory equipped torque assist device that is sized for the higher capacity stage, it is somewhat over sized for the lower stage. This yields a very quick starting time with a relatively unstable removal period. Because both the VFS and the torque assist device are being removed from the circuit at relatively the same time, it is difficult for the VFS to determine when it should start removing capacitance because the torque assist device represents a step change in motor torque and inrush current. Nevertheless, the VFS is able to meet the compensation margin.

5 Ton Two Stage Unit Stage 2 Compensation Margin

The following graphs depict a base line run, in which no compensation was offered, followed by eight consecutive runs on the 5 Ton split system unit running in its higher capacity stage, stage 2. It took the unit four runs to finish tuning to the correct capacitance needed by the unit for the lab impedance. Figures 6.15, 6.16, 6.17, and 6.18 show the RMS voltage, compressor current, capacitor current, and feeder circuit current respectively. A brief discussion of the results continues after the figures.

Figure 6.15. 5-Ton Split System Unit Running in Stage 2 Voltage Measurements.

Figure 6.16. 5-Ton Split System Unit Running in Stage 2 Compressor Current Measurements.

Figure 6.17. 5-Ton Split System Unit Running in Stage 2 Capacitor Current Measurements.

Figure 6.18. 5-Ton Split System Unit Running in Stage 2 Feeder Current Measurements.

The voltage correction as well as starting time is in line with the 2.5 and 4 ton units and the desired results. It is interesting to note that the VFS offers shorter start times even with a unit already equipped with a torque assist device. Again, it is noticed that the feeder current drawn through the branch circuit is still in the general range of the original compressor current. It can also be seen that given more starting time, the VFS responds better to the 5 Ton unit starting in stage 2.

5 Ton Two Stage Unit Alternating Stages

To demonstrate the VFS's compatibility with multistage units, a set of tests were run on the 5-Ton split system unit in which the VFS was initially allowed to tune to the higher stage, stage 2. Then the stage in which the unit started was alternated between stage 1 and stage 2 for several consecutive runs. Since the typical operation of a two stage unit is to allow the lower capacity, more efficient stage to run most of the time with the higher capacity stage used for backup, it is expected that this test is the worst case scenario that the VFS might face in the field. Figure 6.19 shows the RMS voltage measurements from the set of runs.

Figure 6.19. 5-Ton Split System Unit Alternating Stages Voltage Measurements.

In a real world application of a multistage unit, it is expected that the unit will start and run in the lower stage most of the time, utilizing the higher stage for emergencies such as an extremely hot afternoon or chilly night. With respect to the operation of the VFS, this means that it will normally be tuned to the most likely stage to start next, which should be stage 1.

Compensation Level Estimation on the 2.5 Ton Unit

The compensation level estimation test results on the 2.5 Ton unit were obtained by first determining the compensation level according to the worksheet. Table 6.2 contains the measurements and calculation results to obtain the compensation level, which is the estimated feeder voltage drop.

Table 6.2 2.5-Ton Compensation Level Data

Panel Voltage	241.1 V
VFS Voltage	240.0 V
Inrush Current	72 A
Steady State Current	13.5 A
Compensation Level	2.40%

The dip switches are set according to the work sheet, and the actual compensation level used by the controller for this is 2% voltage drop on the branch feeder circuit.

Figures 6.20 and 6.21 show the voltage at the VFS terminals and the false breaker panel, respectively, for an eight run set that allowed for tuning.

Figure 6.20. 2.5-Ton Voltages at the VFS Terminals Given Added Branch Impedance.

Figure 6.21. 2.5-Ton Voltages at the Breaker Panel Given Added Branch Impedance.

Compensation Level Estimation on the 4 Ton Unit

Similarly to the 2.5 Ton test, the compensation level estimation test results on the 4 Ton unit were obtained by first determining the compensation level according to the worksheet. Table 6.3 contains the measurements and calculation results to obtain the compensation level, which is the estimated feeder voltage drop.

Table 6.3 4-Ton Compensation Level Data

Panel Voltage	238.7 V
VFS Voltage	237.6 V
Inrush Current	109 A
Steady State Current	20.5 A
Compensation Level	2.40%

The resulting compensation level is exactly the same as the 2.5 Ton unit, and it is expected that this might not quite be enough to account for the actual voltage drop. The dip switches are set according to the work sheet, and the actual compensation level used by the controller for this is 2% voltage drop on the branch feeder circuit.

Figures 6.22 and 6.23 show the voltage at the VFS terminals and the false breaker panel, respectively, for an eight run set that allowed for tuning.

Figure 6.22. 4-Ton Voltages at the VFS Terminals Given Added Branch Impedance.

Figure 6.23. 4-Ton Voltages at the Breaker Panel Given Added Branch Impedance.

It is clear from these results that the tests on the 4 Ton unit demonstrate the estimated voltage drop used for the compensation level is slightly too small. It should be the next higher level, 2.5% to 2.99%, which would give the controller a level of 2.5% and bring down the slight voltage rise seen at the panel. Nonetheless, it shows that the control scheme works, but a better form of estimation may be required.

Laboratory Testing Discussion

The laboratory testing has shown that the VFS can meet the design goals given the known limitations of the design, including: the initial voltage drop while triggering, the over-voltage as capacitance is removed, and the compensation level estimation scheme. As explained previously, the method of using a full-cycle sliding window RMS calculation to create the representative voltage drop waveforms lends itself to exaggerating the length of short voltage disturbances with respect to a full cycle. The apparently lengthened events lead to a question of whether or not the actual half-cycle voltage drop and removal voltage rise are visible. The question that must be addressed is, do the two events compound upon each other to make the entire compensation interval more visible?

In [7], a study was conducted to determine if positive and negative flashes of light negate or complement each other for a given amount of separation in time. The results of [7] state that the interaction of flashes near threshold that are separated in time compound maximally near 65 ms to twice the individual threshold and the threshold decreases as

interval between the flashes increases. The study also provides evidence that the threshold differences between positive and negative flashes are negligible near the threshold. It can then be concluded that the interaction between the two voltage changes allowed by the VFS during a compensation event will not have a significant compounding effect because the length of the starting event, over 100 ms, is greater than the maxima. Thus it is possible to address the starting voltage drop and the removal voltage rise as individual events.

To address the question of how visible each individual voltage fluctuation is, the differences between the two must be examined. The initial voltage drop while the VFS is triggering is known to be a half-cycle event or 8.3 ms long. From [7], the threshold intensity of a single rectangular flash of this length can be extrapolated to nearly 4 times the calculated threshold in the previously discussed flicker study. This would mean that a voltage drop of 4 % would be nearing the threshold of visibility, with the actual threshold of irritability being well below that. In the worst case scenario from lab testing, the initial voltage drop was found to be around 6 %. This lies near the boundary and it is expected that only the most observant individual could identify this event. Because the initial voltage drop must be present for the VFS to be a nonintrusive device, this cannot be corrected.

In the case of the voltage rise created during the capacitor removal process, the event could possibly be a two and a half cycle or 42 ms long. If this were a continuously modulated event, it would have a frequency of 24 Hz. The IEC/IEEE 1453 standard states that the irritation threshold, $P_{st} = 1$, for sinusoidal and rectangular modulation have

percent allowable voltage fluctuations of 1.365 and 1.072, respectively. Given the worst case scenario seen during compensation margin testing in the lab, the highest routinely seen percent voltage rise was 3 % peak, meaning the voltage rise is over twice that of recommended in [4].

However, the event is not continuously modulated and it is highly unlikely that a flicker meter would register a P_{st} value remotely close to one because averaging the single 42 ms long event over seconds, much less minutes, would significantly reduce its contribution. To further negate the effects of the voltage rise created by the VFS, the results of compensation level testing shows that the added impedances of the branch circuit will create a voltage division effect between the VFS terminals and the actual point of common coupling, the breaker panel. Consequently, the higher the impedance of the branch circuit, the lower the apparent voltage rise seen at the breaker panel.

The compensation level estimation scheme will continue to be improved through either software updates or a better estimation method as the VFS moves into field demonstrations. This is considered continuing work at the time of publication of this thesis.

Summary

In this chapter, the results from laboratory testing were relatively promising in terms of the VFS's ability to correct for voltage flicker. The shortcomings of the data analysis method and design limitations of the VFS were discussed in detail. There is clearly some remaining work to better estimate the panel voltage during field trials.

CHAPTER SEVEN

CONCLUSIONS

Almost everyone has experienced the annoyance of voltage flicker at some point or another in their life and some live with it every day. For the majority of residences, the voltage flicker created by a heat pump compressor starting is hardly visible, but for a few, the voltage drop can be quite significant. The presently commercially available flicker suppression technology, used to alleviate the problem, does not correct for the problem at the root cause. The voltage flicker suppression device has shown that it has the ability to almost completely eliminate visible voltage flicker created by a compressor starting event.

In this thesis, the various aspects of a residential power service associated with voltage flicker are discussed to demonstrate that the VFS's use of shunt capacitance is a viable solution to voltage flicker due to a starting compressor. The usage of small increments of capacitance allows for the VFS to easily adapt its self to nearly any combination of residential heat pump and power service characteristics. The simple but reliable control scheme has proven through lab testing that it is capable of effectively compensating for the voltage flicker while not interfering with the existing HVAC equipment.

Even though there is work to be continued on making the VFS even more reliable and flexible, the present state of the VFS demonstrates that the technology is clearly a feasible solution. The one design goal that the VFS has missed is the total price of the

device, which has come in at over \$500 per unit in small quantities, not including the printed circuit board or the capacitors. The main reason for not meeting the target price is the addition of several costly items to meet NEC® and UL® requirements. The device is not currently UL approved and plans are in motion to have it reviewed by UL® engineers. However, it is hoped that the final VFS, produced on a larger scale, will give power utilities a more cost effective option to address customers' concerns when it comes to voltage flicker.

APPENDICES

Appendix A

Flicker Study Visual Basic Source Code and Screenshots

Figure A.1. Screenshot of the Startup Screen for the Flicker Study.

Figure A.2. Screenshot of the Run Cases Screen for the Flicker Study.

The screenshot shows a software window titled "Flicker Test". It contains several input fields and buttons for configuring a flicker test. At the top, there is a "Test Identifier 'Your User Name'" field with the text "Tester1" and a "Reset Test" button. Below this, there are three main configuration sections: "Duration of Flicker" with a dropdown menu set to "10 cycles" and a "Start Test" button; "Type of Bulbs Used" with radio buttons for "Incandescent" (selected) and "CFL"; and "Type of Sequence" with radio buttons for "Step Out" (selected) and "Ramp Out". A section titled "Choose The Case That Contained The Drop:" contains two buttons, "Case A" and "Case B". At the bottom, there are two small text boxes: the left one says "Your last answer was: CORRECT." and the right one displays the value "117.6".

Flicker Test

Test Identifier "Your User Name"
Tester1

Reset Test

Duration of Flicker
10 cycles

Start Test

Type of Bulbs Used
☒ Incandescent
☐ CFL

Type of Sequence
☒ Step Out
☐ Ramp Out

Choose The Case That Contained The Drop:

Case A Case B

Your last answer was: CORRECT. 117.6

Figure A.3. Screenshot of the Case Selection Screen for the Flicker Study.

```
'-----  
' frmMain  
'  
' Written by: Curtiss Fox  
'  
' Last Updated: 2/11/08  
'  
' Description: These subroutines perform form manipulation, while  
' all calculations are called from the module Sequences.bas  
'
```

```
Private Sub cmdCaseA_Click()
```

```
    CorrectAns False
```

```
    cmdRun.Enabled = True  
    cmdCaseA.Enabled = False  
    cmdCaseB.Enabled = False  
    fraNextStep.Visible = True  
    cmdRun.Visible = True  
    fraChoose.Visible = False  
    cmdCaseA.Visible = False  
    cmdCaseB.Visible = False
```

```
End Sub
```

```
Private Sub cmdCaseB_Click()
```

```
    CorrectAns True
```

```
    cmdRun.Enabled = True  
    cmdCaseA.Enabled = False  
    cmdCaseB.Enabled = False  
    fraNextStep.Visible = True  
    cmdRun.Visible = True  
    fraChoose.Visible = False  
    cmdCaseA.Visible = False  
    cmdCaseB.Visible = False
```

```
End Sub
```

```
Private Sub cmdExample_Click()
```

```
    cmdExample.Enabled = False
```

```
    StartGPIB
```

```
    StartLights
```

```
    runExample
```

```
    StopLights
```

```
    StopGPIB
```

```
End Sub
```

```
Private Sub cmdRun_Click()
```

```
    cmdRun.Enabled = False
```

```
    RunSequence
```

```
    fraChoose.Visible = True
```

```
    cmdCaseA.Visible = True
```

```
    cmdCaseB.Visible = True
```

```
    cmdCaseA.Enabled = True
```

```
    cmdCaseB.Enabled = True
```

```
    fraNextStep.Visible = False
```

```
    cmdRun.Visible = False
```

```
End Sub
```

```
Private Sub cmdStart_Click()
```

```
    ' Ensure Duration Time Selected
```

```
    If cboDuration.ListIndex = -1 Then
```

```
        MsgBox ("Please Select a duration time for this test.")
```

```
        Exit Sub
```

```
    ElseIf optIncand.value = False And optCFL.value = False Then
```

```
        MsgBox ("Please Select a bulb type for this test.")
```

```

Exit Sub
ElseIf optStep.value = False And optRamp.value = False Then
    MsgBox ("Please Select a Sequence Type for this test.")
Exit Sub
ElseIf txtTestName.Text = "" Then
    MsgBox ("Please Enter the Test Identifier as indicated.")
Exit Sub
Else ' Good To GO!

'Disable start button and option changes mid Test
cmdStart.Enabled = False
optIncand.Enabled = False
optCFL.Enabled = False
optStep.Enabled = False
optRamp.Enabled = False
cboDuration.Enabled = False
txtTestName.Enabled = False

frmMain.MousePointer = vbHourglass

'Startup the GPIB and ELGAR
StartGPIB
StartLights

'Initialize Variables in Flicker Module
StartTest

'Show Case start Frame
fraNextStep.Visible = True
fraExample.Visible = False
cmdRun.Visible = True

frmMain.MousePointer = vbDefault

frmMain.SetFocus

End If

End Sub

```

```

Private Sub cmdStop_Click()

    StopTesting False, True

```

End Sub

Private Sub Form_Load()

'Load up the duration combo box
cboDuration.AddItem "5 cycles"
cboDuration.AddItem "10 cycles"
cboDuration.AddItem "15 cycles"
cboDuration.AddItem "20 cycles"

'Ensure all radio buttons are false
optIncand.value = False
optCFL.value = False
optStep.value = False
optRamp.value = False

'Hide Appropriate Items
fraNextStep.Visible = False
fraExample.Visible = True
cmdRun.Visible = False
fraChoose.Visible = False
cmdCaseA.Visible = False
cmdCaseB.Visible = False
txtTestName.Enabled = True
optIncand.value = True
optStep.value = True

End Sub

Private Sub Form_Terminate()

StopLights

StopGPIB

End Sub

Private Sub Form_Unload(Cancel As Integer)

StopLights

StopGPIB

End Sub

Private Sub txtTestName_GotFocus()

txtTestName.SelStart = 0

txtTestName.SelLength = Len(txtTestName)

End Sub

```

'-----
' Sequences.bas
'
' Written by: Curtiss Fox
'
' Last Updated: 2/12/08
'
' Description: This module contains the initialization and sequence
' instructions for communicating with the ELGAR through the GPIB
' port. It will also time the cases and contains the code to determine
' if the correct case was chosen. All required return information is
' set directly to frmMain from this module.
'

```

```

'Declare Global subroutines
Declare Sub Sleep Lib "kernel32" (ByVal dwMilliseconds As Long)
Declare Sub Beep Lib "kernel32" (ByVal dwFreq As Long, ByVal dwDuration As Long)

```

```

'Declare Global Constants
Const GPIB0 = 0 'Interface Card Number
Const ELGAR = 25 'GPIB Address for Elgar
Const gblNomVolts = 120 'Set the nominal voltage level
Const SaveDir = "D:\PQIA\GPIB\Flicker\Data\" 'Save data Dir

```

```

Const intNumReverses = 5 'Add one for the total number of reverses

```

```

'Declare Global Variables

```

```

Dim ApExcel As Object 'To open Excel
Dim intSeqNumber As Integer 'The number of Sequences or Steps run
Dim blCase As Boolean 'The boolean that controls which case is correct (A = false and B
= true)
Dim dblInitStep As Double 'The value of the initial steps
Dim dblFinalStep As Double 'The value of the later steps
Dim blIncandescent As Boolean 'Set if the bulbs used are incandescent, else they are
CFL's
Dim blStep As Boolean 'determines if step or ramp sequence type is chosen
Dim intReverses As Integer 'The number of reverses in the staircase method
Dim blCorrect As Boolean 'Indicates if the last choice was correct
Dim dblCurrentVoltage As Single 'The value of the current step Voltage
Dim strDateTime As String 'Current date and Time MM-DD-hh-mm
Dim dblDeltaV As Double 'The change from the norm of the last lower reverse

```

Sub StartTest()

'Set Current Date and Time of Test for Records

strDateTime = DateTime.Date\$ & "_" & DateTime.Hour(Now) & "-" &
DateTime.Minute(Now)

intSeqNumber = 0

'Set Step sizes In Per Unit

dblInitStep = 0.1

dblFinalStep = 0.02

'Set Initial Starting Point as 5% below Nominal Voltage

dblCurrentVoltage = 0.98 * gblNomVolts

dblDeltaV = gblNomVolts - dblCurrentVoltage

'Pull booleans from main form

blStep = frmMain.optStep.value

blIncandescent = frmMain.optIncand.value

'Initialize global variables

intReverses = 0

blCorrect = False

blCase = False

' Initialize Excel

Set ApExcel = CreateObject("Excel.application") 'Creates an object

ApExcel.Visible = False ' So you can see Excel

ApExcel.workbooks.Add 'Adds a new book.

ApExcel.cells(1, 1).formula = frmMain.txtTestName

ApExcel.cells(2, 1).formula = DateTime.Now

ApExcel.cells(4, 1).formula = "Duration:"

ApExcel.cells(4, 2).formula =

frmMain.cboDuration.List(frmMain.cboDuration.ListIndex())

ApExcel.cells(5, 1).formula = "Step or Ramp:"

If blStep Then

 ApExcel.cells(5, 2).formula = "Step"

Else

 ApExcel.cells(5, 2).formula = "Ramp"

End If

ApExcel.cells(6, 1).formula = "Bulb Type:"

If blIncandescent Then

 ApExcel.cells(6, 2).formula = "Incandescent"

Else

 ApExcel.cells(6, 2).formula = "CFL"

End If

ApExcel.cells(9, 1).formula = "Step #"

ApExcel.cells(9, 2).formula = "Correct Case"

ApExcel.cells(9, 3).formula = "Seq Voltage"

ApExcel.cells(9, 4).formula = "Answer Given"

ApExcel.cells(9, 5).formula = "Correct"

ApExcel.cells(9, 6).formula = "Reverse Number"

ApExcel.Columns("A:F").EntireColumn.AutoFit

End Sub

Sub StartGPIB()

 '=====

 '

 ' INITIALIZATION SECTION

 '

 '=====

 ' Your board needs to be the Controller-In-Charge in order to find all

 ' listeners on the GPIB. To accomplish this, the subroutine SendIFC

 ' is called. If the error bit EERR is set in ibsta, call GpibErr with

 ' an error message.

 Call SendIFC(GPIB0)

 If (ibsta And EERR) Then

 GpibErr ("Error sending IFC.")

 End If

 ' DevClearList will send the GPIB Selected Device Clear (SDC) command

 ' message to all the devices on the bus. If the error bit EERR is set in

 ' ibsta, call GpibErr with an error message.

 Call DevClear(GPIB0, ELGAR)

```

    If (ibsta And EERR) Then
        GpibErr ("Error in clearing the devices. ")
    End If

End Sub

```

```

Sub StopGPIB()

    ilonl GPIB0, 0
    If (ibsta And EERR) Then
        'GpibErr ("Error putting board offline.")
    End If

End Sub

```

```

Sub StartLights()

    'Set Default source voltage to gblNomVolts

    Call Send(GPIB0, 25, "Source:Volt " & CStr(gblNomVolts), NLEnd)
    If (ibsta And EERR) Then
        GpibErr ("Error Sending 'Source Voltage' To Start Lights. ")
    End If

    'Turn the output of the Elgar ON and keep it on

    Call Send(GPIB0, 25, "Output ON", NLEnd)
    If (ibsta And EERR) Then
        GpibErr ("Error Sending 'Output ON'. ")
    End If

End Sub

```

```

Sub StopLights()

    'Turn the output of the Elgar Off and keep it on

    Call Send(GPIB0, 25, "Output OFF", NLEnd)

```

End Sub

Sub RunSequence()

'Declare local Variables

Dim dblStepSize As Double

Dim intCase As Integer

Dim dblCaseVolts As Double

Dim dblCaseBvolts As Double

Dim intCycles As Integer

'### Setup Case Voltages #####

'Determine the step size for this sequence

'If intReverses < 2 Then

' dblStepSize = dblDeltaV * (1 - Exp(intSeqPerRev / dblTauL))

'Else

' dblStepSize = dblFinalStep

'End If

'Determine if we should be moving up or down for this sequence

'If intReverses Mod 2 > 0 Then

' 'Moving Down

' dblStepSize = -dblDeltaV * (1 - Exp(-intSeqPerRev / dblTauL))

'Else

' 'Movin' On Up

' dblStepSize = dblDeltaV * (1 - Exp(-intSeqPerRev / dblTauL))

'End If

'Normalize dblStepSize to Nominal Voltage

'dblStepSize = dblLastRevVolt + dblStepSize

'Calculate Voltage for this Step

'dblCurrentVoltage = dblCurrentVoltage + dblStepSize

dblCurrentVoltage = gblNomVolts - dblDeltaV

'Randomize which case gets the voltage drop

Randomize

intCase = CInt(Int((2 * Rnd()) + 1)) - 1

```

'If Case A
If intCase = 0 Then

    'Set the boolean to False = Case A
    blCase = False

    'Set Voltages for both Cases
    dblCaseAvolts = dblCurrentVoltage
    dblCaseBvolts = gblNomVolts

Else 'Case B

    'Set the boolean to True = Case B
    blCase = True

    'Set Voltages for both Cases
    dblCaseAvolts = gblNomVolts
    dblCaseBvolts = dblCurrentVoltage

End If

' ### Determine Sequence Length #####

Select Case frmMain.cboDuration.ListIndex

    Case 0
        intCycles = 5
    Case 1
        intCycles = 10
    Case 2
        intCycles = 15
    Case 3
        intCycles = 20
    Case Else
        MsgBox ("Error in selecting Cycles")

End Select

' ### Run Sequences #####

'If Step Sequences

```

If blStep Then

StepSeq intCycles, dblCaseAvolts, True
Sleep 1500
StepSeq intCycles, dblCaseBvolts, False

Else 'Ramp Sequences

RampSeq intCycles, dblCaseAvolts, True
Sleep 1500
RampSeq intCycles, dblCaseBvolts, False

End If

'Increment Sequence Number
intSeqNumber = intSeqNumber + 1

'Set Text Box Values for Tester Feedback ++++++
frmMain.optCase.value = blCase
frmMain.txtCurVolt = dblCurrentVoltage

End Sub

Sub CorrectAns(ByVal blAnswer As Boolean)

'See if this answer is CORRECT
If blAnswer = blCase Then

'If moving down and was correct before Reverse directions
' If intReverses Mod 2 > 0 And blCorrect Then
' intReverses = intReverses + 1
' intSeqPerRev = 1
' dblLastRevVolt = dblCurrentVoltage
' dblDeltaV = gblNomVolts - dblCurrentVoltage
' Else
' intSeqPerRev = intSeqPerRev + 1
' End If

'Tell them they are correct
frmMain.txtCorrect.Text = "Your last answer was: CORRECT."


```

If blCorrect Then
    'check to reverse
    If intReverses Mod 2 > 0 Then
        intReverses = intReverses + 1
    End If

    If intReverses < 2 Then
        dblDeltaV = dblDeltaV * (1 - dblInitStep)
    Else
        dblDeltaV = dblDeltaV * (1 - dblFinalStep)
    End If
    'Reset Correct Counter Since that is two in a row
    blCorrect = False

```

```

Else
    'Set correct counter to one
    blCorrect = True
End If

```

```

Else 'Answer is INCORRECT

```

```

    'If moving up and was incorrect last time Reverse Directions
    ' If intReverses Mod 2 = 0 And Not blCorrect Then
    '     intReverses = intReverses + 1
    '     intSeqPerRev = 1
    '     dblLastRevVolt = dblCurrentVoltage
    ' Else
    '     intSeqPerRev = intSeqPerRev + 1
    ' End If

```

```

    'Check to reverse
    If intReverses Mod 2 = 0 Then
        intReverses = intReverses + 1
    End If

```

```

    'Tell them and set it incorrect
    frmMain.txtCorrect.Text = "Your last answer was: INCORRECT."
    blCorrect = False

```

```

    If intReverses < 2 Then
        dblDeltaV = dblDeltaV / (1 - dblInitStep)
    End If

```

```

Else
    dblDeltaV = dblDeltaV / (1 - dblFinalStep)
End If

End If

'Write This Sequence Data to Excel
WriteToExcel blAnswer

'Determine if we are done with the test
If intReverses > 5 Then
    MsgBox "The test is complete. THANKS FOR PLAYING!!! Please Record the Date
and Time as: " & DateTime.Date$ & " " & DateTime.Hour(Now) & ":" &
DateTime.Minute(Now)
    StopTesting False, False
End If

End Sub

```

```

Sub StepSeq(ByVal cycles As Integer, ByVal dblNewVoltage As Double, ByVal
blCaseA)

'Clear the sequence scratch pad

Call Send(GPIB0, 25, "Edit:seq:clear", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Clearing Seg Scratchpad'. ")
End If

'### Create Segment 0 #####
'Buffer Segment to get around the ELGAR Glitch

'Set length of voltage drop in 'cycles'
Call Send(GPIB0, 25, "Edit:seq:cycles 120", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Setting Buffer Seg Cycles'. ")
End If
'Set depth of voltage drop
Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(CCur(gblNomVolts)), NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Source Voltage for Buffer Seg'. ")

```

End If

'### Create Segment 1 #####

'Contains actual voltage step

'Insert segment 1

Call Send(GPIB0, 25, "Edit:seq:insert 1", NLen)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Insert Seg 1'. ")

End If

'Set length of voltage drop in 'cycles'

Call Send(GPIB0, 25, "Edit:seq:cycles " & CStr(cycles), NLen)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Setting Seg 0 Cycles'. ")

End If

'Set depth of voltage drop

Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(CCur(dblNewVoltage)), NLen)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Source Voltage for Seg 0'. ")

End If

'### Create Segment 2 #####

'Will be used as the ending point of the case

'Insert segment 2

Call Send(GPIB0, 25, "Edit:seq:insert 2", NLen)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Insert Seg 2'. ")

End If

'Set segment 1 cycles

Call Send(GPIB0, 25, "Edit:seq:cycles 1", NLen)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Setting Seg 1 Cycles'. ")

End If

'Set segment 1 voltage 'Back to standard voltage'

Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(gblNomVolts), NLen)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Source Voltage for Seg 1'. ")

End If

'### Create Segment 3 #####

'Buffer Segment to get around the ELGAR Glitch

```

'Insert segment 3
Call Send(GPIB0, 25, "Edit:seq:insert 3", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Insert Seg 3'. ")
End If
'Set length of voltage drop in 'cycles'
Call Send(GPIB0, 25, "Edit:seq:cycles 120", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Setting Seg 3 Cycles'. ")
End If
'Set depth of voltage drop
Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(CCur(gblNomVolts)), NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Source Voltage for Seg 3'. ")
End If

'Set mode to run sequence once and stop
Call Send(GPIB0, 25, "Source:seq:mode:run single", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Seq Run Mode Single'. ")
End If
'Set mode to keep voltage at last that of the last segment when sequence is done
Call Send(GPIB0, 25, "Source:seq:mode:stop segment", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Seq Stop Mode Segment'. ")
End If
'Load the sequence from the scratch pad into the buffer
Call Send(GPIB0, 25, "Source:seq:load ""SCRATCH""", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Loading Seq from Scratch Pad'. ")
End If

'Execute the Sequence
Call Send(GPIB0, 25, "Source:seq run", NLEnd)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Running Sequence'. ")
End If

If blCaseA Then

    Sleep 1200
    Beep 1900, 300

```

```
Sleep 1500
Beep 1800, 300
```

```
Else
```

```
Sleep 1200
Beep 1900, 150
Sleep 50
Beep 1900, 150
Sleep 1400
Beep 1800, 150
Sleep 50
Beep 1800, 150
```

```
End If
```

```
End Sub
```

```
Sub RampSeq(ByVal cycles As Integer, ByVal dblNewVoltage As Double, ByVal
blCaseA)
```

```
    'Clear the sequence scratch pad
```

```
    Call Send(GPIB0, 25, "Edit:seq:clear", NLEnd)
```

```
    If (ibsta And EERR) Then
```

```
        GpibErr ("Error Sending 'Clearing Seg Scratchpad'. ")
```

```
    End If
```

```
    '### Create Segment 0 #####
```

```
    'Buffer Segment to get around the ELGAR Glitch
```

```
    'Set length of voltage drop in 'cycles'
```

```
    Call Send(GPIB0, 25, "Edit:seq:cycles 120", NLEnd)
```

```
    If (ibsta And EERR) Then
```

```
        GpibErr ("Error Sending 'Setting Buffer Seg Cycles'. ")
```

```
    End If
```

```
    'Set depth of voltage drop
```

```
    Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(CCur(gblNomVolts)), NLEnd)
```

```
    If (ibsta And EERR) Then
```

```
        GpibErr ("Error Sending 'Source Voltage for Buffer Seg'. ")
```

```
    End If
```

```

'### Create Segment 1 #####
'Contains actual voltage step

'Insert segment 1
Call Send(GPIB0, 25, "Edit:seq:insert 1", NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Insert Seg 1'. ")
End If
'Set length of voltage drop in 'cycles'
Call Send(GPIB0, 25, "Edit:seq:cycles " & CStr(cycles - 3), NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Setting Seg 0 Cycles'. ")
End If
'Set depth of voltage drop
Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(CCur(dblNewVoltage)), NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Source Voltage for Seg 0'. ")
End If

'### Create Segment 2 #####
'Will be used as the ending point of the case

'Insert segment 2
Call Send(GPIB0, 25, "Edit:seq:insert 2", NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Insert Seg 2'. ")
End If
'Set segment 2 cycles
Call Send(GPIB0, 25, "Edit:seq:cycles 3", NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Setting Seg 1 Cycles'. ")
End If
'Set segment 2 to RAMP UP
Call Send(GPIB0, 25, "Edit:seq:sour1:ampl:ramp on", NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Setting Seg 1 Cycles'. ")
End If
'Set segment 3 voltage 'Back to standard voltage'
Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(dblNewVoltage), NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Source Voltage for Seg 1'. ")
End If

```

Create Segment 3

'Will be used as the ending point of the case

'Insert segment 3

Call Send(GPIB0, 25, "Edit:seq:insert 3", NLEnd)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Insert Seg 3'. ")

End If

'Set segment 3 cycles

Call Send(GPIB0, 25, "Edit:seq:cycles 1", NLEnd)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Setting Seg 3 Cycles'. ")

End If

'Set segment 3 voltage 'Back to standard voltage'

Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(gblNomVolts), NLEnd)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Source Voltage for Seg 1'. ")

End If

Create Segment 4

'Buffer Segment to get around the ELGAR Glitch

'Insert segment 3

Call Send(GPIB0, 25, "Edit:seq:insert 4", NLEnd)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Insert Seg 4'. ")

End If

'Set length of voltage drop in 'cycles'

Call Send(GPIB0, 25, "Edit:seq:cycles 120", NLEnd)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Setting Seg 4 Cycles'. ")

End If

'Set depth of voltage drop

Call Send(GPIB0, 25, "Edit:seq:sour1:ampl " & CStr(CCur(gblNomVolts)), NLEnd)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Source Voltage for Seg 4'. ")

End If

'Set mode to run sequence once and stop

Call Send(GPIB0, 25, "Source:seq:mode:run single", NLEnd)

If (ibsta And EERR) Then

 GpibErr ("Error Sending 'Seq Run Mode Single'. ")

```

End If
'Set mode to keep voltage at last that of the last segment when sequence is done
Call Send(GPIB0, 25, "Source:seq:mode:stop segment", NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Seq Stop Mode Segment'. ")
End If
'Load the sequence from the scratch pad into the buffer
Call Send(GPIB0, 25, "Source:seq:load ""SCRATCH""", NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Loading Seq from Scratch Pad'. ")
End If

'Execute the Sequence
Call Send(GPIB0, 25, "Source:seq run", NLen)
If (ibsta And EERR) Then
    GpibErr ("Error Sending 'Running Sequence'. ")
End If

If blCaseA Then

    Sleep 1200
    Beep 1900, 300
    Sleep 1500
    Beep 1800, 300

Else

    Sleep 1200
    Beep 1900, 150
    Sleep 50
    Beep 1900, 150
    Sleep 1400
    Beep 1800, 150
    Sleep 50
    Beep 1800, 150

End If

End Sub

```

```

Sub StopTesting(ByVal blcritical As Boolean, ByVal blUserReset)

```



```

'Determine if an error was thrown by GPIB or ELGAR and ask them to record message
If blcritical Then
    MsgBox "An Error has ocured and the Test will be Reset. Please Record the
following Error Messages for me.", vbCritical
Else 'Else it was a correct termination
    If blUserReset Then
        SaveExcel True
    Else
        SaveExcel False
    End If
End If

```

```

'Unload and reload main form to reset test
Unload frmMain
Load frmMain
frmMain.Visible = True

```

```

End Sub

```

```

Sub WriteToExcel(ByVal blAnswer As Boolean)

```

```

'Local Variable to index excel rows
Dim index As Integer
index = intSeqNumber + 9

```

```

'Fill in the columns on the excel sheet
ApExcel.cells(index, 1).formula = intSeqNumber

```

```

If Not blCase Then
    ApExcel.cells(index, 2).formula = "A"
Else
    ApExcel.cells(index, 2).formula = "B"
End If

```

```

ApExcel.cells(index, 3).formula = CStr(CCur(dblCurrentVoltage))

```

```

If Not blAnswer Then
    ApExcel.cells(index, 4).formula = "A"
Else
    ApExcel.cells(index, 4).formula = "B"
End If

```

```

If blCase = blAnswer Then
    ApExcel.cells(index, 5).formula = "X"

```

End If

ApExcel.cells(index, 6).formula = intReverses

End Sub

Sub SaveExcel(ByVal blInComplete)

'Save Excel sheet and release excel

If blInComplete Then

 ApExcel.activeworkbook.saveas SaveDir & frmMain.txtTestName.Text & " " &
 strDateTime & "_NC.xls"

 ApExcel.activeworkbook.Close

Else

 ApExcel.activeworkbook.saveas SaveDir & frmMain.txtTestName.Text & " " &
 strDateTime & ".xls"

 ApExcel.activeworkbook.Close

End If

ApExcel.quit

Set ApExcel = Nothing

End Sub

Sub runExample()

'Declare local Variables

Dim dblStepSize As Double

Dim intCase As Integer

Dim dblCaseVolts As Double

Dim dblCaseBvolts As Double

Dim intCycles As Integer

Dim dblExampleVolts As Double

' ### Setup Case Voltages #####

dblExampleVolts = 0.98 * gblNomVolts

```

'Randomize which case gets the voltage drop
Randomize
intCase = CInt(Int((2 * Rnd()) + 1)) - 1

'If Case A
If intCase = 0 Then

    'Set the boolean to False = Case A
    blCase = False

    'Set Voltages for both Cases
    dblCaseAvolts = dblExampleVolts
    dblCaseBvolts = gblNomVolts

Else 'Case B

    'Set the boolean to True = Case B
    blCase = True

    'Set Voltages for both Cases
    dblCaseAvolts = gblNomVolts
    dblCaseBvolts = dblExampleVolts

End If

' ### Determine Sequence Length #####

intCycles = 15

' ### Run Sequences #####
'Step Sequences

    StepSeq intCycles, dblCaseAvolts, True
    Sleep 1500
    StepSeq intCycles, dblCaseBvolts, False

Sleep 1000

frmMain.cmdExample.Enabled = True
End Sub
Private Sub GpibErr(msg$)

```

```

'Start StopTesting
StopTesting True, False

'Throw the error message hopefully someone will pay attention to
msg$ = msg$ + AddIbsta() + AddIberr() + AddIbcnt() + Chr(13) + Chr(13) + "I'm
quitting!"
MsgBox msg$, vbOKOnly + vbExclamation, "Error"

' Take the board offline.

iln! GPIB0, 0

End
End Sub

```

```

Private Function AddIbcnt() As String
    AddIbcnt = Chr$(13) + Chr$(10) + "ibcnt = 0x" + Hex$(ibcnt)
End Function

Private Function AddIberr() As String

    If (ibsta And EERR) Then
        If (iberr = EDVR) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = EDVR <DOS
Error>"
        If (iberr = ECIC) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ECIC <Not
CIC>"
        If (iberr = ENOL) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ENOL <No
Listener>"
        If (iberr = EADR) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = EADR
<Address Error>"
        If (iberr = EARG) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = EARG <Invalid
argument>"
        If (iberr = ESAC) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ESAC <Not Sys
Ctrlr>"
        If (iberr = EABO) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = EABO <Op.
aborted>"
        If (iberr = ENEB) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ENEB <No
GPIB board>"
        If (iberr = EOIP) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = EOIP <Async
I/O in prg>"
        If (iberr = ECAP) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ECAP <No
capability>"

```

```

    If (iberr = EFSO) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = EFSO <File sys.
error>"
    If (iberr = EBUS) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = EBUS
<Command error>"
    If (iberr = ESTB) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ESTB <Status
byte lost>"
    If (iberr = ESRQ) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ESRQ <SRQ
stuck high>"
    If (iberr = ETAB) Then AddIberr = Chr$(13) + Chr$(10) + "iberr = ETAB <Table
overflow>"
    Else
        AddIberr = Chr$(13) + Chr$(10) + "No error, iberr = " + Str$(iberr)
    End If
End Function

```

Private Function AddIbsta() As String

```

    sta$ = Chr$(13) + Chr$(10) + "ibsta = &H" + Hex$(ibsta) + " <"
    If (ibsta And EERR) Then sta$ = sta$ + " ERR"
    If (ibsta And TIMO) Then sta$ = sta$ + " TIMO"
    If (ibsta And EEND) Then sta$ = sta$ + " END"
    If (ibsta And SRQI) Then sta$ = sta$ + " SRQI"
    If (ibsta And RQS) Then sta$ = sta$ + " RQS"
    If (ibsta And CMPL) Then sta$ = sta$ + " CMPL"
    If (ibsta And LOK) Then sta$ = sta$ + " LOK"
    If (ibsta And RREM) Then sta$ = sta$ + " REM"
    If (ibsta And CIC) Then sta$ = sta$ + " CIC"
    If (ibsta And AATN) Then sta$ = sta$ + " ATN"
    If (ibsta And TACS) Then sta$ = sta$ + " TACS"
    If (ibsta And LACS) Then sta$ = sta$ + " LACS"
    If (ibsta And DTAS) Then sta$ = sta$ + " DTAS"
    If (ibsta And DCAS) Then sta$ = sta$ + " DCAS"
    sta$ = sta$ + ">"
    AddIbsta = sta$
End Function

```

Appendix B

NEC Installation Requirements and Panel Voltage Estimation

Example Normalized Inrush Voltage Drop Estimation Worksheet

Instructions: Before beginning, ensure that safe points of measurement are available on the 240V circuit at both the breaker panel and HVAC exterior pull disconnect. With the compressor running, measure both the breaker panel voltage and the voltage at the disconnect. Record these values in the space provided.

$V_{\text{Breaker Panel}} =$ _____

$V_{\text{Disconnect}} =$ _____

Determine the normalized voltage drop by dividing the disconnect voltage by the breaker panel voltage and subtracting the result from 1. The result must be less than 1. Record this value in the space below.

$$V_{\text{Normalized}} = 1 - \left(\frac{V_{\text{Disconnect}}}{V_{\text{Breaker Panel}}} \right) = \underline{\hspace{2cm}}$$

From the nameplate of the compressor, record the ratings for the compressor's RLA and LRA in the space provided.

$I_{\text{RLA}} =$ _____

$I_{\text{LRA}} =$ _____

Find the ratio of the inrush current by dividing the LRA by the RLA. The result must be larger than 1. Record this value in the space provided.

$$\text{Inrush Ratio} = \frac{I_{\text{LRA}}}{I_{\text{RLA}}} = \underline{\hspace{2cm}}$$

To find the final normalized inrush voltage drop on the branch circuit, multiply the normalized voltage by the inrush ratio. Find this value in the table below.

$$V_{\text{DropInrush}} = (V_{\text{Normalized}}) * (\text{Inrush Ratio}) = \underline{\hspace{2cm}}$$

Normalized Inrush Voltage Drop Table

Calculated Inrush Voltage	S1	S2	S3	S4
0 - 0.49	OFF	OFF	OFF	OFF
0.5 - 0.99	ON	OFF	OFF	OFF
1 - 1.49	OFF	ON	OFF	OFF
1.5 - 1.99	ON	ON	OFF	OFF
2 - 2.49	OFF	OFF	ON	OFF
2.5 - 2.99	ON	OFF	ON	OFF
3 - 3.49	OFF	ON	ON	OFF
3.5 - 3.99	ON	ON	ON	OFF

Calculated Inrush Voltage	S1	S2	S3	S4
4 - 4.49	OFF	OFF	OFF	ON
4.5 - 4.99	ON	OFF	OFF	ON
5 - 5.49	OFF	ON	OFF	ON
5.5 - 5.99	ON	ON	OFF	ON
6 - 6.49	OFF	OFF	ON	ON
6.5 - 6.99	ON	OFF	ON	ON
7 - 7.49	OFF	ON	ON	ON
7.5 - 8	ON	ON	ON	ON

Use the sequence for the given voltage drop range to set the corresponding dip switches on the VFS.

- **VFS Enclosure**
 - Size: TBD
 - Material: ABS
 - Mounting: Wall Mount
 - Type: NEMA 3 (or equivalent)
 - Door: Hinged
- **VFS Power Conductors**
 - Between the VFS and the HVAC Disconnect and Cap Stages: Use #10 AWG, 600 V, three conductors (L1, L2, and Gnd).
 - Between VFS and HVAC Unit: Use existing wiring infrastructure. Emphasis on minimal modification.
- **VFS Fusing**
 - Use 250V, 30A and 20A, slow-blow type (TRM 20 and TRM 30 or equivalents).
 - One fuse per capacitor stage.
 - 20 A for 300 μ F stage.
 - 30 A for the 600 and 900 μ F stages
- **VFS Disconnect**
 - Use a 240V, 60A Non-automatic Switch (QOU200 or equivalent).
- **VFS Discharge Resistors**
 - 34 k Ω of less for 900 μ F stages.
 - 52 k Ω of less for 600 μ F stage.
 - 104 k Ω of less for 300 μ F stage.
- Use flexible, armor conduit and weatherproof fittings between the VFS and HVAC Disconnect.
- Use appropriate compression lugs and ferrules for all power conductor terminations. No unterminated power conductors!
- Use appropriate compression lugs on sense wires as applicable.

Figure B.1. The NEC® Installation Requirements.

Appendix C

VFS Bill of Materials

Printed Circuit Board (Active)

Item	MFG	MFG Part #	Quantity / Unit	Cost / Unit
Microcontroller	Microchip	DSPIC30F3013-30I/SP	1	\$7.75
Power TRIAC	Teccor	Q4040K7	6	\$40.98
Pilot TRIAC	Fairchild	FOD420	6	\$14.28
5V DC Regulator	Fairchild	LM7805CT	1	\$0.45

Printed Circuit Board (Passive)

Item	MFG	MFG Part #	Quantity / Unit	Cost / Unit
Transformer (240 / 2 x 18V)	Tamura	PL5.0-36-130B	1	\$7.30
Current Transformer	CR Magnetics	CR8349-2500-N	1	\$11.20
Rectifier Diodes (Schottky 1A 40V Axial)	ON Semi	1N5819G	12	\$5.16
Zener Diodes (5.1 V at 3 W Axial)	ON Semi	1N5338BG	2	\$0.00
Resistors (10 Ohms 1/4 W Axial)			2	\$0.00
Resistors (18 Ohms 1/4 W Axial)			1	\$0.00
Resistors (240 Ohms 1/4 W Axial)		Standard Stocked Items	1	\$0.00
Resistors (1 k Ohms 1/4 W Axial)		All 1/4 W Resistors are	4	\$0.00
Resistors (1.1 k Ohms 1/4 W Axial)		assumed 0.3" pitch	1	\$0.00
Resistors (1.5 k Ohms 1/4 W Axial)			7	\$0.00
Resistors (10 k Ohms 1/4 W Axial)			6	\$0.00
Resistors (380 Ohms 1/2 W Axial)	Vishay	SFR16S0003900FR500	6	\$1.31
Resistor (3.3 k Ohms 2 W Axial) Bleeders	Vishay	PR02000203301JR500	6	\$3.62
Capacitor (100 uF 50V Radial)	Panasonic	EEU-FC1H101	1	\$0.44
Capacitor (10 uF 50V Radial)	Panasonic	ECA-2AHG100	1	\$0.30
Capacitor (0.33uF 50V Radial)	CDE	167334J63A	1	\$0.66
Capacitor (0.1uF 50V Radial)	Kemet	C320C104K5R5TA	7	\$1.47
MOV (240V)	Littelfuse	TMOV20R275E	1	\$1.66
MOV (120V)	Littelfuse	TMOV20R150EP	2	\$3.44

PCB Connectors

Item	MFG	MFG Part #	Quantity / Unit	Cost / Unit
Power Connector (3 pin socket)	Molex	10-84-4030	1	\$0.83
Power Connector (3 pin plug)	Molex	50-84-1030	1	\$0.28
Screw Terminals	Keystone	8197	12	\$4.48
CT Connector Male	Molex	22-03-2031	2	\$0.70
LED and Reset Connector Male	Molex	22-03-2021	2	\$0.38
CT Connector Female (3 pin 0.1" space)	Molex	22-01-2037	2	\$0.40
LED and Reset Connector Female	Molex	22-01-2027	2	\$0.26
Connector Terminals 22-30AWG	Molex	08-50-0114	10	\$1.24
Connector Terminals 14-20AWG	Molex	02-08-1002	3	\$0.26
28 Pin Dip Socket (PIC)	3M	4828-3004-CP	1	\$0.33
8 Pin Dip Socket (Dip switches)	Assmann	A08-LC-TT-R	1	\$0.32
6 Pin Dip Socket (Pilot Triacs)	Assmann	A06-LC-TT-R	6	\$3.54

Enclosure and Disconnect

Item	MFG	MFG Part #	Quantity / Unit	Cost / Unit
Enclosure Non-metallic (14 x 12 x 6)	Hubbell	HW-J141206CHQR	1	\$75.00
Backplane (Aluminum)	Hubbell	HW-MP1412A	1	\$11.25
Disconnecting Switch	SquareD	QOU200	1	\$68.69
Switch Mounting Feet	SquareD	QOUMF2B	2	\$2.84
Switch Rain-proof cover	SquareD	BCV	1	\$22.17
Push Button Reset Switch SPST-NO	Tyco	MSPS103C0	1	\$2.39
PCB Standoffs (1/2 ")	Keystone	1893	10	\$4.35
900 uF Mounting Bracket	CDE	VR10A	4	\$10.04
300 uF Mounting Bracket	CDE	VR8	3	\$6.81

Terminal Blocks and Wiring

Item	MFG	MFG Part #	Quantity / Unit	Cost / Unit
Screw Clamp Terminal Block	Phoenix Contact	3006043	10	\$46.60
Term Block Separating Plate	Phoenix Contact	3003224	3	\$3.03
Term Block Fixed Bridges	Phoenix Contact	0203454	1	\$12.92
Term Block End Brackets	Phoenix Contact	1201442	4	\$4.36
Ring Crimp Terminals (10 AWG 1/4" ring)	Tyco	35110	24	\$6.96
Ring Crimp Terminals (16 AWG 1/4" ring)	Tyco	31894	12	\$2.76
14 AWG Quick Disconnect	Molex	19007-0021	4	\$1.32
18 AWG Quick Disconnect	Molex	19007-0001	4	\$1.00
10 AWG Red (3 feet)				
10 AWG Black (3 feet)		Minimum Supply On Hand		
14 AWG Red (3 feet)		High strand count		
14 AWG Black (3 feet)		to increase flexibility		
14 AWG Green (3 feet)				
CT, Reset Switch, and LED Indicator (28 AWG)		Standard Stocked Item		

Protection

Item	MFG	MFG Part #	Quantity / Unit	Cost / Unit
30 A 11/32' Fuse Clips	Keystone	3566	80 On Hand	\$0.00
10 A 5x20mm Fuse Clips	Keystone	3519	90 On Hand	\$0.00
15 Amp Slo-Blow Fuses	Ferraz Shawmut	TRM15	2	\$5.80
30 Amp Slo-Blow Fuses	Ferraz Shawmut	TRM30	4	\$12.40

Total / Unit **\$413.73**

Figure C.1. Initial VFS Enclosure Layout Full View.

Figure C.2 Top View of the VFS PCB and Terminal Blocks.

Figure C.3. Final Enclosure Layout Front View.

Figure C.4. Final Enclosure Layout Open View.

Appendix D

Microcontroller Source Code

```
//-----  
//  
//      VSD Controller Code for the dsPIC30F3013  
//  
//      Written by: Curtiss Fox  
//  
//      Last Updates: 9/17/08  
//  
//      Description: This program will allow for the specified microcontroller  
//      to operate the VSD within a 1% correction margin.  
//      The set points are for a 70A trigger current used with a classic 'doughnut'  
//      style CT. The cutoff voltage is set to 100.5%  
//-----  
  
#include "p30F3013.h"  
#include <libpic30.h>  
  
//PIC specific Setups  
_FWDTC(WDT_OFF); //WatchDog OFF  
_FOSC(CSW_FSCM_OFF & FRC & FRC_PLL16); //Fast internal RC clk at 16x (~30 Mhz)  
_FBORPOR(MCLR_DIS & PBOR_ON & BORV_27 & PWRT_OFF); //Disable Master Clear and set Brown-out voltage  
  
// ++++++++ CONSTANTS ++++++++  
  
//Set a Placeholder for EEPROM Data by initializing a row vector up front  
long _EEDATA(32) fooArrayInDataEE[] = {0,0,0,0,0,0,0};  
  
//Stage Definitions w/ 1/3 stages  
const int StageB[16] =  
{0x0000,0x0000,0x0000,0x0080,0x0080,0x0080,0x00C0,0x00C0,0x00C0,0x01C0,0x01C0,0x01C0,0x03C0,0x03C0,0x03C0,0x03C0  
};  
const int StageF[16] =  
{0x0000,0x0020,0x0010,0x0000,0x0020,0x0010,0x0000,0x0020,0x0010,0x0000,0x0020,0x0010,0x0000,0x0020,0x0010,0x0030};  
  
//Current Constants  
const int OnCurrentPos =      411;                // 70 Amps (1100 on CR8348-2000)  
const int OffCurrentPos      =      30;           // 5 Amps averaged over a half cycle (80 on  
CR8348-2000)  
  
//Cutout Voltage gain constant  
const float TurnOffGain =      1.007;             //Turn off at 100.7% Voltage  
  
//Tuning Constants  
const float switchCompGain = 0.0003;             //The voltage drop for each switch is 0.3%  
const float compLevelGain = 0.005;              //The level gain is 0.5% per step  
  
// ++++++++ VARIABLES ++++++++  
  
//Declare Variables : Controller  
signed int ADResultC = 0;                        //Current Sample  
unsigned int ADResultV = 0;                      //Voltage Sample  
unsigned long ADSumC = 0;                        //Current Sum  
signed long LastSumC[3] = {0,0,0};              //Last two Current Sums  
  
unsigned long ADSumV = 0;                        //Voltage Sum  
unsigned long LastSumV[3] = {0,0,0};            //Last two Voltage Sums
```

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unsigned long PreVoltage[3] = {0,0,0};          //PreStart Voltage
unsigned long TurnOffVoltage[3] = {0,0,0}; //PreStart Voltage

unsigned long PostVoltage[3] = {0,0,0};         //PostStart Voltage
unsigned long InVoltage[3] = {0,0,0};          //Insert Voltage
unsigned long InCurrent[3] = {0,0,0};          //Insert Current
unsigned long InitCurrent[3] = {0,0,0};        //Initial Current

unsigned int EvenCycle = 0;                     //Holds the even/odd cycle counter
unsigned int samples = 0;                      //Samples during this half cycle
unsigned int OnCycle = 0;                      //Number of cycles caps are on

unsigned int OnCycleSet = 40; //Number of desired cycles caps are on in HALF CYCLES (40 = 20 full cycles)
unsigned int OutputB = 0x0000;                //PortB output
unsigned int OutputF = 0x0000;                //PortF output

unsigned int Control = 0x0000; //Control register to signify events during starting
unsigned int OnCurrentSamples = 0; //Sample number to eliminate dv/dt current spikes

unsigned int StartUpTimer = 0;
unsigned int DelayTimer = 0;

unsigned long fooArrayinRAM[8] = {0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0};
unsigned int StartCycles = 0;

//Declare Variables : TuneUp
double PreStartV = 0;
double InStartV = 0;
double deltaVi = 0; //Used to Calculate the Stages needed

int switchComp = 0;
int compLevel = 0;
double compCurrent = 0;

double VswitchComp = 0;
double VcompLevel = 0;
double VdiffActual = 0;

unsigned long TotalStages = 0; //Used to Hold the Total stages
unsigned int WorkingStages = 0; //Used to Hold the Working stages
unsigned int TuneStages = 0; //Used to Hold the Current Tune Stages stages

int main(void)
{

//Initialize the Controller=====

//Input Initialization

ADPCFG = 0b111111111001111; //Make AN4 and AN5 analog, rest digital

//Note to self, read and set LATCH before TRIS

LATB = 0x0000; //Latch PortB at 0 before turn on
TRISB = 0xC3F; //Turn PortB 6-9 to output, use the rest as inputs (A/D and DI)

LATF = 0x0000; //Latch PortF at 0 before turn on
TRISF = 0x0000; //Turn all of PortF output

LATD = 0x0100; //Latch RB8 high LED
TRISD = 0x0200; //Turn RB9 to input

//RESET OPTION ++++++

```

```

//Declare pointer for EEPROM data
_prog_addressT EE_addr;
//Initialize the variable to represent the Data EEPROM address */
_init_prog_address(EE_addr, fooArrayInDataEE);

if (PORTDbits.RD9 == 1) {

    // RESET ++++++

    //Set Working variables to initial states ( zero )
    TotalStages = 0;
    InitCurrent[0] = 0;
    InitCurrent[1] = 0;

    //Set Working Variables for capacitor stages
    WorkingStages = TotalStages;
    TuneStages = TotalStages % 3;

    //Copy To working Variables into the Array to write to EEPROM
    fooArrayinRAM[0] = TotalStages;
    fooArrayinRAM[1] = InitCurrent[0] ;
    fooArrayinRAM[2] = InitCurrent[1];

    /*Erase a row in Data EEPROM at array "fooArrayinDataEE" */
    _erase_eedata(EE_addr, _EE_ROW);
    _wait_eedata();

    /*Write a row to Data EEPROM from array "fooArraylinRAM" */
    _write_eedata_row(EE_addr, (int *)fooArrayinRAM);
    _wait_eedata();

    //Timer Setup for Delay (30 Seconds)
    TMR2 = 0; // Clear timer 2 register
    TMR3 = 0; // Clear timer 3 register
    PR2 = 0x5A4E; // Least Significant Period
    PR3 = 0x0003; // Most Significant Period
    IFS0bits.T3IF = 0; // clr interrupt flag
    IEC0bits.T3IE = 1; // set interrupt enable bit
    T2CON = 0x8038; // Fosc/4, 1:256 prescale, 32 bit, start TMR2

    LATD = 0x0100; //Turn off RB8 LED

    //Flash for waiting
    TMR1 = 0; // clear timer 1
    PR1 = 0x3938; // Set Period for 2 seconds
    IFS0bits.T1IF = 0; // clr interrupt flag
    IEC0bits.T1IE = 1; // set interrupt enable bit
    T1CON = 0x8030; // Fosc/4, 1:256 prescale, start TMR1

    //Wait for 30 second timeout
    while(DelayTimer == 0);

    //Reset Delay Flag
    DelayTimer = 0;

    //Turn off RB8 LED
    LATD = 0x0100;

    //Clear Timers
    T1CON = 0x0000;
    T2CON = 0x0000;

}else { //Copy over the data from the EEPROM

    // RESTART ++++++

```



```

//Copy array "fooArrayinDataEE" from DataEEPROM to "fooArrayinRAM" in RAM*/
_memcpy_p2d16(fooArrayinRAM, EE_addr, _EE_ROW);

//Copy To working Variables in the program space
TotalStages = fooArrayinRAM[0];
InitCurrent[0] = fooArrayinRAM[1];
InitCurrent[1] = fooArrayinRAM[2];

//Set Working Variables for capacitor stages
WorkingStages = TotalStages;
TuneStages = TotalStages % 3;

}

// AD CONFIGURATION

//AD config reg 1
ADCON1bits.FORM = 0; //Set integer output
ADCON1bits.SSRC = 7; //Start Conversion automatically
ADCON1bits.ASAM = 1; //Start on Sample Bit being set

//AD config reg 2
ADCON2bits.VCFG = 0;
ADCON2bits.CSCNA = 1;
ADCON2bits.SMPI = 1;
ADCON2bits.BUFG = 0;
ADCON2bits.ALTS = 0;

//AD config reg 3
ADCON3bits.SAMC = 12;
ADCON3bits.ADCS = 1;
ADCON3bits.ADRC = 0;

//AD channel select register
ADCHS = 0x0000;

//AD Channel scan select register
ADCSSL = 0b0000000000110000; //Sample AN4 and AN5 (V and I respectively)

//Turn AD ON
ADCON1bits.ADON = 1;

while(1) { //Loop Endlessly%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

//Ready State While Loop
while((Control & 0xFFFF) != 0x0FFF){

//Check on A/D
while(!IFS0bits.ADIF);

//Increase samples this time
samples++;

//Get A/D buffer data: Classic CT
ADResultC = ADCBUF1;
ADResultV = ADCBUF0;

//Add to the half cycle sums
ADSumC = ADSumC + ADResultC;
ADSumV = ADSumV + ADResultV;

//Set to Turn on the caps if the current is high enough
if ((ADResultC > OnCurrentPos) && (Control & 0x00FF) == 0x0000) {

```

```

//Do only if we are over the number of samples to eliminate dv/dt current spikes for striking
if (OnCurrentSamples > 30) {
    //Compressor is now ON and set caps to TURN ON at next HALF CYCLE
    Control = Control | 0x000F;

    //Check for cold load pickup by making sure both half cycle voltages are greater than
    setpoint

    if (StartCycles >= 3) {
        //Get PreVoltages
        PreVoltage[0] = LastSumV[0];
        PreVoltage[1] = LastSumV[1];
        PreVoltage[2] = LastSumV[2];
        //Set Turn off Gains : Moved Calculation to In Voltage
        //TurnOffVoltage[0] = LastSumV[0] * TurnOffGain;
        //TurnOffVoltage[1] = LastSumV[1] * TurnOffGain;
    } // Else use EEPROM Values
} else {
    OnCurrentSamples++;
}

}

//Half Cycle Loop
+++++
if (ADResultV < 0x0200 && samples > 60){

    //Update Average Voltage and Clear Averages
    LastSumV[EvenCycle] = ADSumV/samples;
    LastSumC[EvenCycle] = ADSumC/samples;
    LastSumV[2] = samples;

    //Know that the compressor is OFF, RESET CONTROL, and turn off TMR1
    if ((Control & 0x00FF) == 0x00F0) {
        if (LastSumC[EvenCycle] < OffCurrentPos) {
            Control = 0x0000;
            T1CON = 0x0000;
        }
    } else {
        LATD = LATD ^ 0x0100;
    }

    //Increment Start Cycles
    if (StartCycles <= 3) {
        StartCycles++;
    }

    //Clear Half Cycle Variables
    samples = 0;
    ADSumV = 0;
    ADSumC = 0;

    //Switch Control : Turn ON ++++++
    if (((Control & 0x00FF) == 0x000F) && (OnCycle < OnCycleSet)) {
        //Set Compressor On Flag leave fired ON
        Control = 0x00FF;
        //Increment On Cycle Counter
        OnCycle++;
        //Set Output
        LATB = StageB[WorkingStages];
        LATF = StageF[WorkingStages];
    } else if ((Control & 0x00FF) == 0x00FF) {
        OnCycle++;
    }

    // Turn OFF ++++++ Controlled ++++++

```

```

OnCycle >=6 ) {

    if ((Control & 0x00FF) == 0x00FF && LastSumV[EvenCycle] > TurnOffVoltage[EvenCycle] &&

        //Remove Tuning Stages : Remove Tuning and first Full stage
        if(TuneStages > 0 && WorkingStages > 3) {
            WorkingStages = WorkingStages - TuneStages;
            //WorkingStages = WorkingStages - 3;
            LATB = StageB[WorkingStages];
            LATF = StageF[WorkingStages];
            TuneStages = 0;
        }
        //Remove Full Stages
        }else if (WorkingStages >= 3) {
        //if (WorkingStages >= 3 ) {
            WorkingStages = WorkingStages - 3;
            LATB = StageB[WorkingStages];
            LATF = StageF[WorkingStages];
        }
        //Remove Last Stage
        }else if (WorkingStages < 3){
            LATB = StageB[0];
            LATF = StageF[0];
            Control = 0x0FFF;
        }

    }

    // Turn OFF ++++++ STOP ALL ++++++
    if ((Control & 0x0FFF) == 0x00FF && OnCycle >= OnCycleSet) {
        //Set Output Low
        LATB = 0x0000;
        LATF = 0x0000;
        //Set Control to POST and leave compressor ON
        Control = 0x0FFF;
    }
    //If Switch Control END

    //Capture The Starting Voltage and Current
    if (OnCycle == 4){
        //Copy Starting Current
        InVoltage[0] = LastSumV[0];
        InVoltage[1] = LastSumV[1];
        InVoltage[2] = LastSumV[2];

        //Set Turn off Gains ++++++
        TurnOffVoltage[0] = LastSumV[0] * TurnOffGain;
        TurnOffVoltage[1] = LastSumV[1] * TurnOffGain;

        //Copy Starting Voltage
        InCurrent[0] = LastSumC[0];
        InCurrent[1] = LastSumC[1];
        InCurrent[2] = LastSumC[2];
    }

    //Increment Cycle
    EvenCycle = EvenCycle ^ 0x0001;

    }//If Half Cycle End ++++++

} //End While =====

//CleanUp Control Variables on EXIT
OnCycle = 0;
Control = 0x00F0; //Compressor is still on
LastSumV[2]=0;
LastSumC[2]=0;
ADSumV = 0;
ADSumC = 0;

```

```

//Stages tuneup =====

//If no capacitance inserted, record starting current

//If no Caps inserted, recapture the initial current
if (TotalStages == 0) {
    InitCurrent[0] = InCurrent[0];
    InitCurrent[1] = InCurrent[1];
}

//If not a cold load pickup, take it as a useful run
if( PreVoltage[0] > 0 && PreVoltage[1] > 0) {

    //Calculate the voltage difference seen by the VFS
    PreStartV = PreVoltage[0] + PreVoltage[1];
    InStartV = InVoltage[0] + InVoltage[1];
    VdiffActual = InStartV/PreStartV;

    //Calculate the switch offset voltage
    //=====
    //One switch for each full stage
    switchComp = TotalStages / 3;
    //Check if a tuning stage is present, then add 1
    if (TotalStages % 3 > 0) {
        switchComp = switchComp + 1;
    }
    //Check for the all six stages on condition
    } else if (TotalStages == 15) {
        switchComp = (TotalStages / 3) + 2;
    }

    VswitchComp = switchComp * switchCompGain;

    //Calculate the Compensation level voltage drop
    //=====
    //Clear Compensation Level
    compLevel = 0;
    //Set Compensation level based on DIP Switches
    if (PORTBbits.RB3 == 0){
        compLevel = compLevel + 1;
    }
    if (PORTBbits.RB2 == 0){
        compLevel = compLevel + 2;
    }
    if (PORTBbits.RB1 == 0){
        compLevel = compLevel + 4;
    }
    if (PORTBbits.RB0 == 0){
        compLevel = compLevel + 8;
    }
    //Calculate the current ratio of the apparent voltage drop
    if ( InitCurrent[0] > 0 && InitCurrent[1] > 0 ) {
        compCurrent = (InCurrent[0] + InCurrent[1]) / (InitCurrent[0] + InitCurrent[1]) ;
    } else { //Should Never Happen, but used as a catch all
        compCurrent = 1;
    }

    //Calculate the compensation level voltage based on the desired gain
    VcompLevel = compLevel * compLevelGain * compCurrent;

    //Calculate the final effective estimate of the panel voltage
    deltaVi = 1 - (VdiffActual + VswitchComp + VcompLevel);

```

```

//Set new TotalStages based on deltaVi
if (deltaVi > 0.030) { //Accelerated Gain
    TotalStages = TotalStages + 3;
} else if (deltaVi > 0.0125) { //Simple Gain
    TotalStages++;
} else if (deltaVi < 0.000) { //Negative Gain
    TotalStages--;
}

//Ensure TotalStages is within practical limits
if (TotalStages > 15) {
    TotalStages = 15;
} else if (TotalStages < 0) {
    TotalStages = 0;
}

//Set Working Variables for capacitor stages
WorkingStages = TotalStages;
TuneStages = TotalStages % 3;

//Copy To working Variables into the Array to write to EEPROM
fooArrayinRAM[0] = TotalStages;
fooArrayinRAM[1] = InitCurrent[0];
fooArrayinRAM[2] = InitCurrent[1];

/*Erase a row in Data EEPROM at array "fooArrayinDataEE" */
_erase_eedata(EE_addr, _EE_ROW);
_wait_eedata();

/*Write a row to Data EEPROM from array "fooArray1inRAM" */
_write_eedata_row(EE_addr, (int *)fooArrayinRAM);
_wait_eedata();

} //End if real correction attempt or just cold start

//Set Working Variables for capacitor stages
WorkingStages = TotalStages;
TuneStages = TotalStages % 3;

//End Stages TuneUp

//Timer Setup for Delay after Compressor Starting (30 Seconds)
TMR2 = 0; // Clear timer 2 register
TMR3 = 0; // Clear timer 3 register
PR2 = 0x5A4E; // Least Significant Period
PR3 = 0x0003; // Most Significant Period
IFS0bits.T3IF = 0; // clr interrupt flag
IEC0bits.T3IE = 1; // set interrupt enable bit
T2CON = 0x8038; // Fosc/4, 1:256 prescale, 32 bit, start TMR2

LATD = 0x0100; //Turn off RB8 LED

//Flash for waiting
TMR1 = 0; // clear timer 1
PR1 = 0x3938; // Set Period for 2 seconds
IFS0bits.T1IF = 0; // clr interrupt flag
IEC0bits.T1IE = 1; // set interrupt enable bit
T1CON = 0x8030; // Fosc/4, 1:256 prescale, start TMR1

//Wait for 30 second timeout
while(DelayTimer == 0);

//Reset Delay Flag
DelayTimer = 0;

```

```

//Turn off RB8 LED
LATD = 0x0100;

//Clear Timers
T1CON = 0x0000;
T2CON = 0x0000;

} //Return to Ready State %%%%%%%%%%%
return 0;
}

//Interrupt for Timer 1 (StartUp Timer)
void __attribute__((interrupt, no_auto_psv)) _T1Interrupt(void)
{
    IFS0bits.T1IF = 0;           // clear interrupt flag

    LATD = LATD ^ 0x0100;

    StartUpTimer = 1;
}

//Interrupt for Timer 3 (Delay Timer)
void __attribute__((interrupt, no_auto_psv)) _T3Interrupt(void)
{
    T2CON = 0x0000;
    IFS0bits.T3IF = 0;           // clear interrupt flag
    DelayTimer = 1;
}

```

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