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THE ELECTRICAL CHARACTERIZATION OF TANTALUM CAPACITORS AS MIS DEVICES

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THE ELECTRICAL CHARACTERIZATION OF TANTALUM CAPACITORS AS MIS DEVICES

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ABSTRACT

Electrical characteristics of a new class of tantalum capacitor are presented. Specifically, this type of tantalum capacitor is manufactured by KEMET Electronics Corporation and utilizes Poly(3,4-ethylenedioxythiolphene) (PEDOT) as the cathode material. There are two capacitor varieties based on the polymerization method used for the PEDOT. One uses In-Situ polymerization, and the other uses Pre-Polymerization. Existing polymer Ta capacitors use In-Situ polymerization while Pre-Polymerization is a new technique of cathode application. We investigated both types of devices to determine what, if any, performance benefits were gained by using Pre-Poly.

In a basic form Ta capacitors consist of a Ta anode, Ta_2O_5 dielectric, and PEDOT cathode polymerized to be a semiconductor. Based on the simplified representation of the capacitor materials these devices were investigated as MIS structures and C-V, I-t, and I-V measurements were made. C-V measurements were used to observe characteristics of MIS operation in the devices. Measurements were made from room temperature down to 100K in attempts to suppress the leakage current in these devices. I-t and I-V measurements were used to identify dominating leakage current mechanisms. The Poole-Frenkel Effect, the Schottky Effect, and Space-Charge-Limited Current were observed in In-Situ polymerized devices, while the Poole-Frenkel Effect, the Schottky Effect, and Fowler-Nordheim Tunneling were observed in Pre-Poly devices. Overall, both devices showed voltage dependent capacitance. The Pre-Poly devices generally had lower levels of leakage current. However, due to differing properties of the polymer in each case In-Situ devices exhibited less capacitance loss at low temperatures.

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CHAPTER ONE

INTRODUCTION

1.1 Tantalum Capacitors

Solid tantalum capacitors have been an integral component in electronics over the past few decades. Their compact construction and large capacitance makes them volumetrically efficient. This volumetric efficiency is one of the main reasons they are an ideal choice in many applications such as portable electronics equipment. As the technologies they support grow by leaps and bounds, so too must tantalum capacitors themselves. High reliability and high frequency applications necessitate constant improvements in all materials associated with tantalum capacitors. One of the current improvements includes changing the cathode material to a semiconducting polymer, yielding significant reliability and performance gains. It is devices using this specific improvement that we will refer to as modern tantalum capacitors. Improvements such as these not only help to meet new performance demands, but also to stay competitive with other types of capacitors.

1.2 Summary of Chapters

In Chapter 2 we discuss an overview of basic capacitor models for parallel plate and electrolytic capacitors. We also use the basic parallel plate model to make generalizations about the capacitance in more complex structures.

In Chapter 3 we introduce the tantalum capacitor and review its historical evolution into its present form. The detailed structure of tantalum capacitors and how

they are manufactured leads into some of their main reliability and performance issues. As with any technology, there must be constant improvement and evolution in order to stay competitive.

In Chapter 4 we present and review modern tantalum capacitors in which we see the first major materials change in tantalum capacitor composition in several decades with the addition of an inherently conducting polymer (ICP) cathode. By examining the materials of this new capacitor system, we show that this type of capacitor can be viewed as an MIS system. We then conduct a basic review of fundamental MIS theory, introducing the basic modes of operation of an MIS device. A literature review of tantalum-based MIS devices is also presented in this chapter.

In Chapter 5 we review some basic conduction mechanisms including the Poole-Frenkel Effect, Space-Charge-Limited Current, Fowler-Nordheim Tunneling, and the Schottky Effect. These mechanisms represent a list of possible sources of dc leakage current in modern tantalum capacitors.

In Chapter 6 we present the results of several different types of measurements, including Capacitance-Voltage measurements, Current-Time measurements, and Current-Voltage measurements. These measurements are conducted on two types of modern tantalum capacitors, with varying levels of performance of each type. All of the measurements are performed in a manner similar to how they would be performed for an MIS device, and we intended to classify modern tantalum capacitors as such. The results of these measurements are qualitative but show similarities to MIS theory, and the results identify conduction mechanisms present in each device.

In Chapter 7, the final chapter, we summarize our results, what goals were achieved, and ideas for future research on modern tantalum capacitors.

CHAPTER TWO

REVIEW OF GENERAL CAPACITOR THEORY

2.1 Parallel Plate Capacitors

The simplest model of a capacitor consists of two parallel metal plates or electrodes separated by a dielectric. Charge is stored on these conductive plates; the positively charged plate is known as the anode, and the negatively charged plate is the cathode. As the electric field across the dielectric increases, so does the charge, giving rise to a potential difference that increases proportionally to the charge. The ratio of the magnitude of the charge to the magnitude of the potential difference between the plates is defined as the capacitance of a capacitor, and for a parallel plate device this can be written as,

$$C = \frac{\Delta Q}{\Delta V} = \frac{\kappa \varepsilon_0 A}{d} \tag{2.1}$$

where;

ΔQ = Charge stored on a single plate

ΔV = Potential difference between the two plates

κ = Dielectric constant

ε_0 = Permittivity of vacuum

A = Plate area

d = Distance between plates, or the dielectric thickness

Because the potential difference increases proportionally to the stored charge, the ratio of $Q/\Delta V$ is constant for a given capacitor. Therefore, capacitance is a measure of a capacitor's ability to store charge. The capacitance depends mainly on plate geometry and the properties of the dielectric. As seen in Equation (2.1), capacitance is directly proportional to the area of the conductive plates and inversely proportional to the distance between them. It is also directly proportional to the dielectric constant of the material separating the plates [1,2].

For any dielectric material there is a maximum electric field that can be applied while still maintaining insulating properties. This is known as the dielectric strength of the material. Beyond this point the dielectric begins to breakdown and conduct current. In a capacitor with a determined dielectric thickness, the dielectric strength is met at a specific applied voltage known as the breakdown voltage. Exceeding the breakdown voltage can cause permanent damage or fatal destruction to the capacitor. The breakdown voltage represents the upper limit of operation for a capacitor. Under normal circumstances devices are not operated near this point, but within a range known as the working voltage range. The working voltage is defined by the capacitor manufacturer to be the maximum voltage at which the capacitor can be operated, and still retain its intended level of performance [3].

2.2 Electrolytic Capacitors

Another common type of capacitor is the electrolytic capacitor, which is often used in applications where large amounts of charge are needed at relatively low voltages. Electrolytic capacitors are classified as such due to the fact that either one or both of the

conductive plates is an electrolyte. An electrolyte is typically a solution that conducts electricity via the ions contained within the solution. The dielectric in an electrolytic capacitor is formed from the anode material itself. In the formation process, the anode, typically a metal, is placed in an electrolyte bath while current flows through the anode to the bath cathode [3]. This current flow causes an oxidation of the anode surface, creating a thin oxide film that perfectly matches the contours of the anode surface [4]. In the case of a parallel plate capacitor, a flat plate, for the cathode electrode, would be placed in contact with the dielectric to complete the capacitor structure. However, since the chemically formed dielectric of the electrolytic capacitor is a very rough, thin, and fragile surface, this is not possible. Contact from the dielectric to the cathode plate must then be made through a medium that can conform to the dielectric surface. The most common material for this purpose is a liquid electrolyte. The structure of an electrolytic capacitor is illustrated in Fig 2.1 [4].

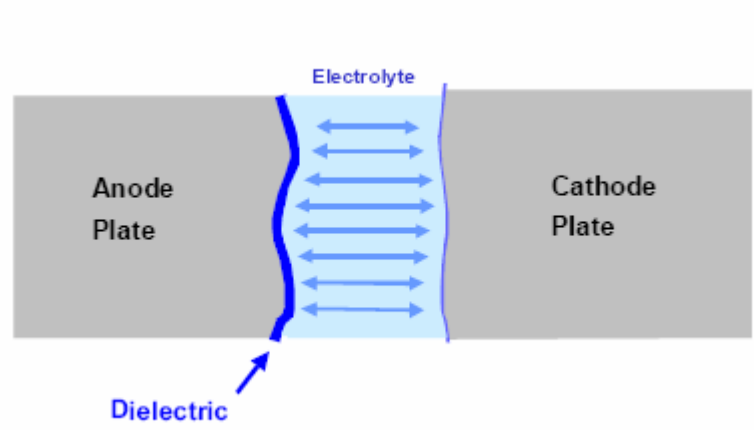

Fig 2.1 Electrolytic Capacitor – Cathode plate extension through electrolyte.

Electrolytes have a lower conductivity than metals and therefore are only used in situations such as this when direct contact to a metal is not possible. A benefit from using a medium, such as a liquid electrolyte, is that ionic current through the electrolyte helps to maintain the integrity of the dielectric by healing any dc leakage sites through reformation of the dielectric in a fashion similar to how it was originally formed [1]. The main advantages of electrolytic capacitors are that they provide a large amount of capacitance in a small package — this is known as volumetric efficiency — and are cost efficient when compared to their parallel plate counterparts [1]. While electrolytic capacitors are more complex than parallel plate capacitors, according to Fig 2.1 the plate electrodes are still essentially parallel. The cathode plate is effectively connected to the dielectric, through the electrolyte medium, therefore the use of Equation (2.1) to describe these devices is still valid. Upon re-examining Equation (2.1), it is easily seen how the properties of electrolytic capacitors, those that necessitate the use of an electrolyte, benefit the overall capacitance of these devices. By increasing the effective surface area of each of the plates as well as decreasing the oxide thickness between them, large amounts of capacitance can be achieved [1,3].

2.3 Conclusion

In this chapter parallel plate and electrolytic capacitors were reviewed. The model for a parallel plate capacitor was used to show how generalizations can be made to predict how capacitance is affected by the components of more complex capacitors. The electrolytic capacitor was introduced as a more complex type in which the parallel plate

model can still be applied. In the next chapter a very specific type of electrolytic capacitor, using tantalum as its anode, will be discussed.

CHAPTER THREE

TANTALUM CAPACITORS

3.1 Evolution of Tantalum Capacitors

Electrolytic capacitors are often the optimum choice in situations where large amounts of capacitance are required, due to their benefits discussed in Chapter 2. Historically electrolytic capacitors were used heavily for by-pass, blocking, and power-supply filter applications as well as for motor starting purposes. However, the low electric quality and reliability associated with these capacitors limited their applications in the area of electronics, often forcing users to resort to bulky costlier types of capacitors [5].

The development of the tantalum anode yielded significant improvements over previous aluminum anodes due to the high dielectric constant of tantalum oxide and the chemical stability of both tantalum and its oxide. The switch to tantalum increased the range of operating temperatures and allowed the use of electrolytic solutions of high conductivity and low freezing point. Despite these improvements, there were still several limitations associated with all wet electrolytic capacitors, such as the large amount of volume occupied by the electrolyte, container, and hermetic seal; the low temperature limitations resulting from solidification of the electrolyte; and a limited shelf life [4,5]. The main benefit of using a wet electrolyte solution is that the liquid electrolyte conforms to the dielectric surface and allows the dielectric reformation process at fault sites. But, even this benefit had the drawback of using a caustic solution, which can generate gases and cannot withstand the thermal cycles of a surface mount assembly [6].

The next advancement in these capacitors came not from tantalum but from the cathode with which it was paired. The tantalum solid electrolytic capacitor was a new type of break-through in electrolytic capacitors. It contained no liquids of any kind and was composed of stable, inorganic, nonvolatile materials. Instead of the traditional liquid electrolyte, a manganeous nitrate solution was applied as the cathode plate connection through a series of dips, with drying cycles in between dips. The result was that the dielectric layer was coated with manganese dioxide (MnO_2), a semiconducting solid [6]. The chemical deposition of MnO_2 allowed the cathode plate connection to conform to the dielectric surface, but with a completely solid structure. Tantalum capacitors now required much less volume for packaging, no longer needed a hermetic seal, had much better temperature characteristics, and a longer shelf life [5].

Once solid tantalum capacitors had been successfully developed, the market began to demand smaller devices at lower prices. Progress in packaging technology made it possible to encapsulate solid tantalum capacitors in an epoxy resin. Due to their superior performance over aluminum electrolytic capacitors, as well as their small size, these resin-type devices had a huge impact on the consumer electronics market. There were two ways in which solid tantalum capacitors continued to develop. The first was through improvements in the packaging; the other was through the improvement of capacitor elements such as dielectric film and MnO_2 dielectric coverage [7].

The price of raw tantalum rose drastically between 1979 and 1982 causing the price of solid tantalum capacitors to no longer be competitive against aluminum electrolytic and other comparable capacitors. The reaction by manufacturers was to

reduce the amount of tantalum per capacitor as much as possible without reducing the rated capacitance. As a result, advances in high-capacitance tantalum powders were utilized. By using fine powders, a much larger overall surface area was achieved allowing equal performance while using much less raw material. The benefit was reduced size and cost of solid tantalum capacitors [7].

The reduction in size and cost of the solid tantalum capacitors halted their replacement by other types; however, designers were still reluctant to use them for fear of future price increases. The next technological advancement was the development of the molded chip-type packaging, which enabled solid tantalum capacitors to be easily applied to surface mount technologies. Solid tantalum capacitors have a much higher resiliency to heat than do other electrolytic capacitors, giving them a huge advantage in this area. Continuing advances in tantalum powders helped to increase the capacitance while holding the case size constant for chip-type solid tantalum capacitors, thus continually increasing the volumetric efficiency of these devices [7,8].

Portable electronic equipment has become a huge market, causing a need for low power, portable, digital, and safe electronics. This placed a new set of demands on solid tantalum capacitors. In order to keep up with the technology it supports, solid tantalum capacitors must be even more compact and store more charge. Also, it is necessary for them to have a low working voltage for power saving purposes, operate at high frequencies, and have high reliability for safety reasons. With these new sets of challenges, the evolution of the tantalum capacitor is beginning to take another turn with the use of inherently conducting polymers (ICPs) for the cathode plate material [8]. The

aim of this shift in materials is to keep the solid state benefits achieved with MnO_2 while removing its associated undesirable traits as a cathode plate contact [9].

3.2 Construction

The construction of tantalum capacitors begins with a fine tantalum powder. This powder traditionally has been a spherical grain that has been shrinking in diameter with improved manufacturing processes. This is according to the industry trend of increasing volumetric efficiency by having higher capacitance in the same or smaller package. To accomplish this, the surface area within a given volume must be increased by using a finer tantalum particle size. Recent developments have also shown the possibility of using tantalum flakes instead of spheres [6]. Either way, all developments in tantalum powders move in the direction of increasing surface area, or capacitance per unit volume.

The anode of the capacitor is formed from tantalum powder by pressing it into a pellet around a tantalum wire. This pellet is a compact collection of the tantalum particles. Within the pellet there is a large amount of open volume. As the particles are pressed together their spherical geometry creates point contacts, electrically connecting them while leaving large gaps and channels between particles. The tantalum wire creates a common electrical contact for all tantalum particles within the pellet [9].

The pellet now has a tantalum wire surrounded by tantalum powder. At this point there are finite contacts between all the particles and the wire, and these contacts are weak. The pellet is then sintered in a vacuum at extremely high temperatures to expand the bond areas of each contact point. This process decreases the volume of the pellet slightly but ensures electrical connection between all the grains as illustrated in Fig 3.1.

The sintering process also helps to drive out any contaminants that were introduced during the pressing process. After sintering, the pellet is essentially pure tantalum. All particles are now electrically connected, and there is still a tremendous amount of voids and channels between particles. This porous nature of the tantalum pellet is what gives solid tantalum capacitors such large amounts of surface area within a confined volume [6,9].

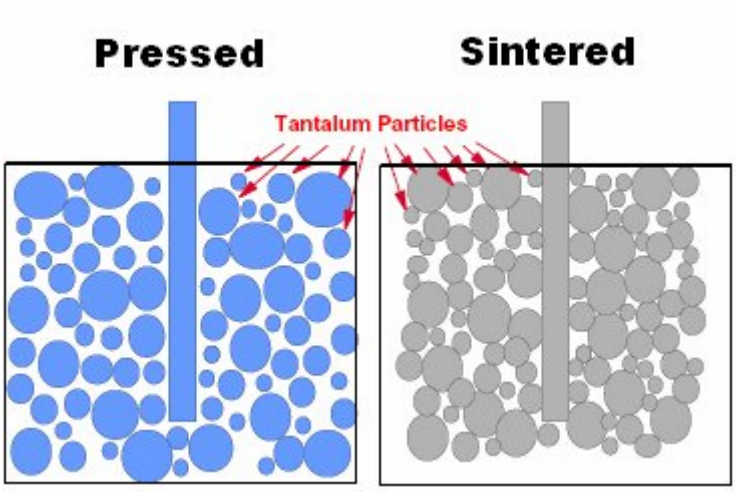

Fig 3.1 Tantalum Pellet after pressing and sintering [9].

Now that the anode is complete, the next step in the process is to cover all exposed surfaces of tantalum metal with a dielectric layer. This is accomplished by submersing the pellet into an electrolyte bath and passing current through the system. The liquid electrolyte fills all the voids and channels and makes contact with the tantalum particles and wire. Oxygen from the electrolyte then combines with tantalum to form an oxide. The type of oxide is determined by electrolyte selection, and the desired outcome is tantalum pentoxide (Ta_2O_5). The thickness and consistency of the oxide layer is

determined by the time, current, and formation voltage applied during the process. As the dielectric forms, it grows to support the formation voltage, and the overall thickness is approximately 18 angstroms per volt of formation voltage [6,9].

At this point an electrolytic capacitor exists as the tantalum pellet is separated from the electrolyte bath by a dielectric layer. The construction of a wet tantalum capacitor would replace the bath electrolyte with one more suitable to perform the task of making contact with the cathode plate. The benefit of having a wet electrolytic capacitor is that the dielectric can fail at any one point and the electrolytic solution will allow reformation of the dielectric. This reformation process is a necessary benefit in electrolytic capacitors because the dielectric layer can have deficiencies due to underlying impurities in the anode metal. Once the dielectric layer is formed, there will always be defects that exist within it regardless of the processes that follow. Using an electrolyte without reformation properties or depositing a conductive material directly on the oxide will lead to high leakage current and capacitors that do not function due to electrical shorts [9].

The cathode material must be applied in liquid form in order to penetrate all the voids and channels that have been formed. The pellet is dipped in a solution of $MnNHO_3$ which comes into contact with all of the exposed surfaces of Ta_2O_5 within and around the pellet. Next, the pellet is heated to dry the solution and convert it to MnO_2. This "dip and dry" step is repeated until there is a thick and continuous coating of MnO_2 in contact with the dielectric [4,6]. MnO_2 is a solid material with a unique property. Its highest oxide form (MnO_2) is also its most conductive and is used for the cathode plate contact.

However, high amounts of current passing through the material can cause an elevated temperature which leads to a conversion to a lower oxide state (Mn_2O_3) that also dramatically increases the resistivity of the material [9].

At this point MnO_2 penetrates into the pellet and covers all of its outside surfaces. On top of the MnO_2 a silver paint is applied to allow a low-resistance external connection to the capacitor. But before the silver is applied, a coating of graphite solution is applied to eliminate interfacial resistances due to contact and silver oxide formation at the interfacial region. The pellet is then cured with heat to dry the graphite and silver solutions [4]. The construction of the capacitor up to this point is illustrated in Fig 3.2.

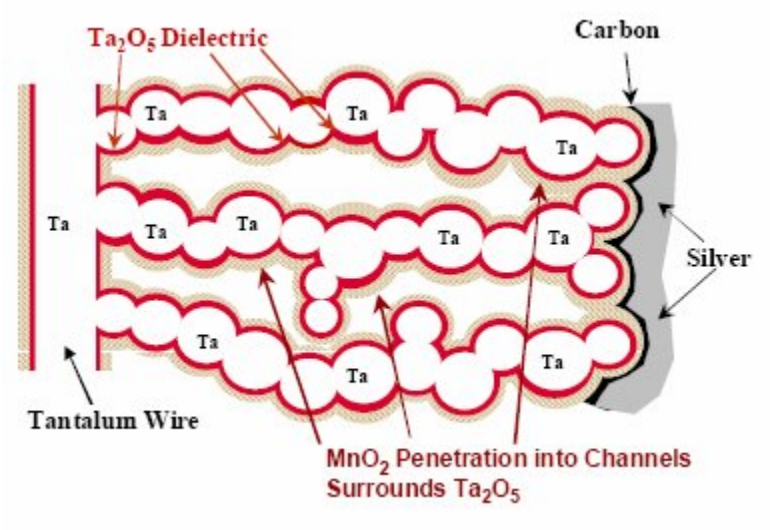

Fig 3.2 Anode and cathode plate structures in tantalum pellet [4].

A lead-frame is then connected to the silver paint with conductive epoxy, to make an external cathode connection, while the tantalum wire is welded to another lead-frame element to make the external anode connection. The final step in the manufacturing process is to seal the entire capacitor in molded plastic while allowing the lead-frames to

extend out of the mold to make external contacts [9]. An illustration of a completed chip-type solid tantalum capacitor can be seen in Fig 3.3.

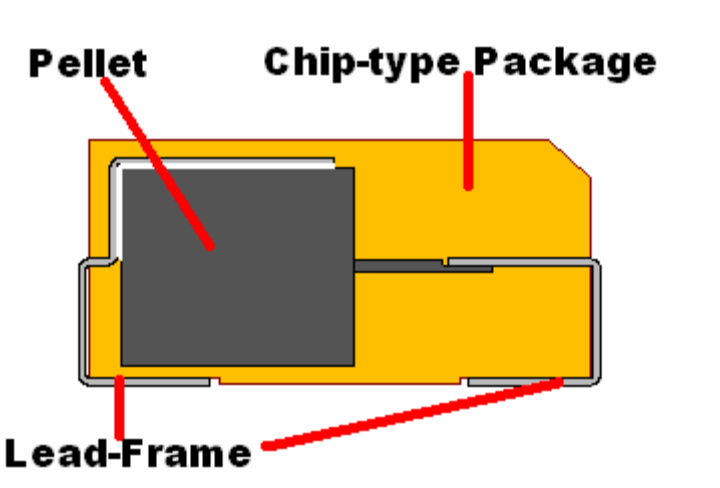

Fig 3.3 Completed chip-type solid tantalum capacitor.

3.3 Reliability Issues

It is common practice within the realm of solid tantalum capacitors for manufacturers to recommend a 50% de-rating for these devices. This means that even though a capacitor is rated for a certain operational voltage, manufacturers recommend no more than half that voltage be used in practical applications. The reasoning behind this recommendation is an attempt to limit turn-on and infant mortality failures to a reasonable level.

One key contributor to these early failures is thought to be stress-induced defects in the dielectric. In cases such as in Fig 3.4, MnO_2 is deposited inside small channels and openings within the tantalum pellet. When MnO_2 is deposited, it is a very hard and brittle layer on top of the dielectric. The cathode formation process involves dipping the pellet in a manganese nitrate solution at around room temperature, followed by the conversion

of this solution to a solid material at around 270°C. To ensure complete coverage, this process is repeated many times. All of the materials within the capacitor are inherently different and have varying coefficients of thermal expansion. These differences can create mechanical stress and ultimately lead to cracks in the dielectric. Any crack or defect in the dielectric layer will be a likely source of leakage current and possible failure in these capacitors [10].

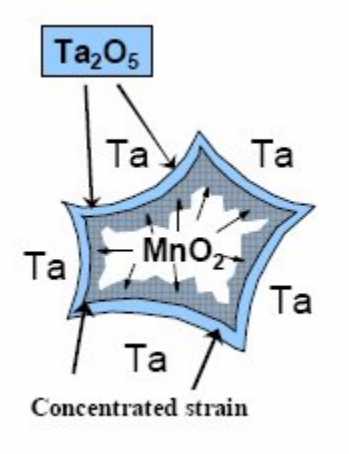

Fig 3.4 MnO_2 as contributing force to cracks [4].

It is impossible to create a capacitor with a perfect and continuous dielectric film. There are degrees of impurities found in the tantalum metal and formation electrolyte solution even when dealing with the most pure of materials [11]. These impurities may be in the low parts per billion range, but due to the enormous dielectric surface area of these devices, it only takes one fault site to create a debilitating current [4]. These impurities, along with stressed areas created during processing, create weakened or undeveloped sites within the dielectric. When exposed to a voltage stress, these sites collapse and allow current to flow through what is intended to be an insulating layer [9].

When a site in the dielectric begins to conduct current, the local MnO_2 in contact with that point will begin to heat up. This current will eventually create enough heat localized in one point in the MnO_2 layer to cause conversion to a lower oxide level (Mn_2O_3). As previously discussed, this conversion dramatically increases the resistivity of the material, restricting the current through the fault site enough to effectively shut it off. This effect is referred to as "self-healing," although leakage sites are not actually healed as they are in liquid electrolytic capacitors, but are merely removed from the system. This process is illustrated in Fig 3.5, in which a dielectric crack and a nickel impurity cause fault sites [4,9].

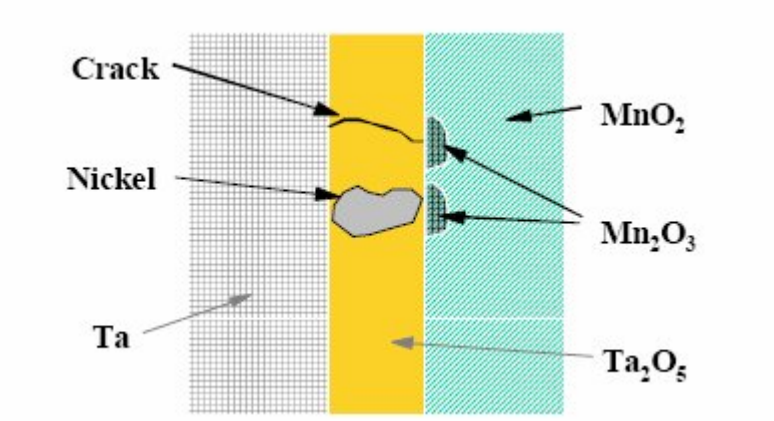

Fig 3.5 MnO_2 self-healing properties [4].

Every solid tantalum capacitor that is manufactured is stressed, prior to sale, by an applied bias in order to activate this self-healing mechanism. This process is known as aging the capacitor. As voltage is applied to these capacitors, more fault sites are removed causing the leakage current to decrease. This phenomenon will continue to take place, beyond the aging period, as application life increases [9].

While the self-healing abilities of MnO_2 are the saving grace for solid tantalum capacitors, these same mechanisms can also lead to its catastrophic failure. Self-healing only requires sufficient current and time for the proper conversions to take place. If the current is insufficient, not enough heat will be generated to heal the site. If the current being conducted at the fault site is very high, the dielectric will begin to heat up at the same time as the MnO_2 [4]. At a temperature slightly higher than that required for self-healing, the dielectric will convert from an amorphous to a crystalline structure. This crystalline conversion begins at the fault site and spreads out across the dielectric, eliminating any previously healed sites. The tantalum at the fault site begins to heat and rapidly absorb any excess oxygen, reaching an exothermic reactive state in the presence of an abundant supply of oxygen. The heated MnO_2 readily supplies the excess oxygen, as it converts to its lower oxide state, feeding this reaction which is commonly referred to as ignition, illustrated in Fig 3.6 [4,9,11].

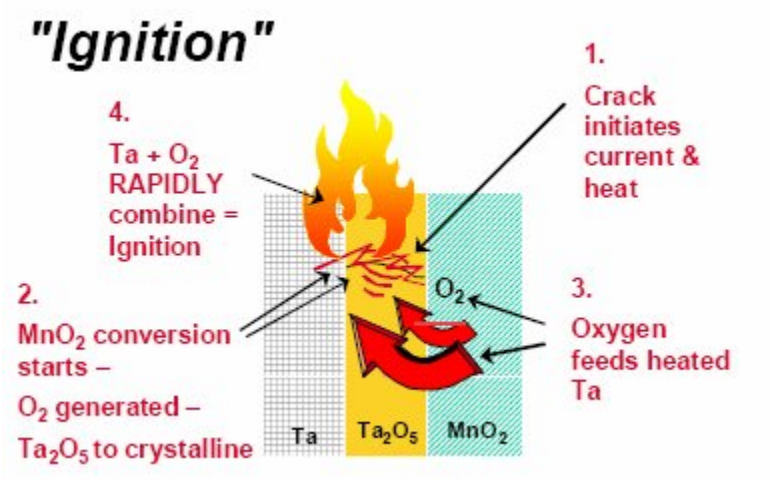

Fig 3.6 Theoretical ignition failure sequence [4].

The ignition reaction not only causes significant failure in these devices, but does so in a very visible fashion as shown in Fig 3.7. MnO_2 and its self-healing mechanisms are the primary reason that solid tantalum capacitors are widely used in practice. However, the abundance of oxygen in MnO_2 also readily supplies solid tantalum capacitors with a source of failure.

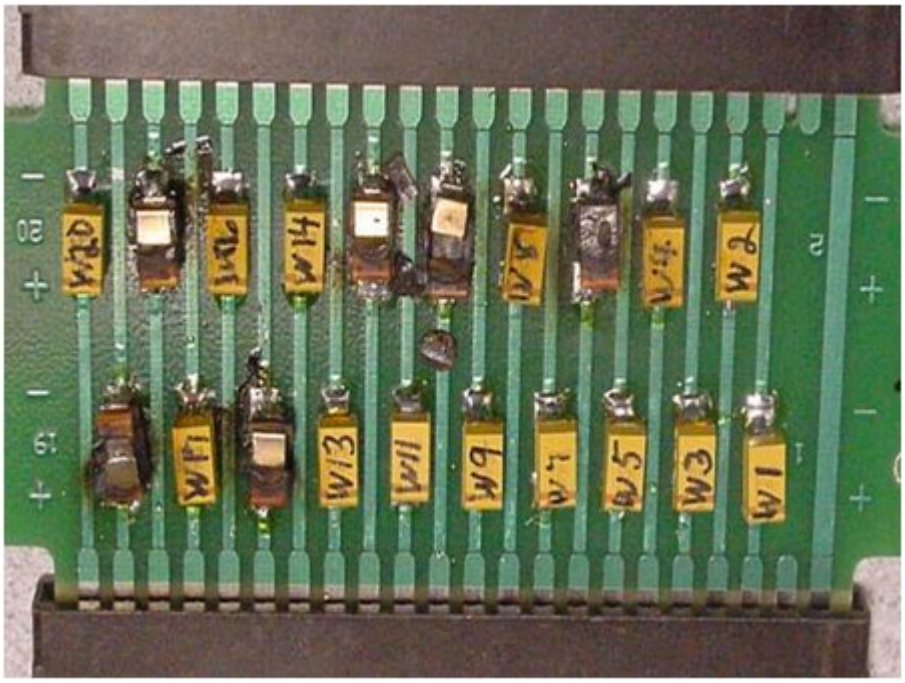

Fig 3.7 Visible ignition failures [12].

3.4 Electrical Performance

All capacitors have certain parasitic elements. Equivalent series resistance (ESR) exists due to the fact that the plates of the capacitor are not perfect conductors as well as the loss associated with the dielectric. Equivalent series inductance (ESL) is created when current is restricted to follow a defined physical path. The current must be crowded into the available paths, and greater restriction over a longer path increases the ESL. A

general view of the electrical performance of a capacitor can usually be represented as a series arrangement of its capacitance along with ESR and ESL as in Fig 3.8. Many of the parasitic elements are determined not only by the choice of materials, but by how those materials are packaged during manufacturing. Different choices in materials or processes will lead to changes in the parasitic elements of these capacitors [4].

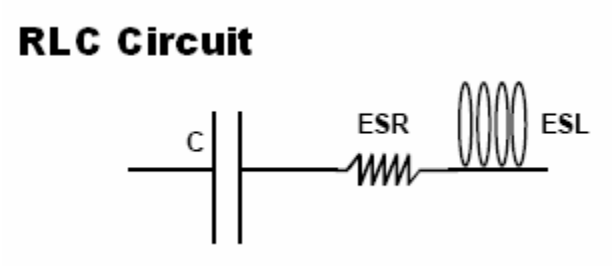

Fig 3.8 RLC Circuit representation of a capacitor [4].

During the construction of solid tantalum capacitors, tantalum powder is pressed and sintered to form a pellet. This structure creates a distributed capacitive network, illustrated in Fig 3.9, with the tantalum particles as the connecting anode media and the MnO_2 as the connecting cathode media. This arrangement creates an increase in resistance to the elements located closer to the center of the pellet structure [4].

The representation of capacitor structure now becomes a complex RC-Ladder of capacitive elements made from individual tantalum particles and their associated resistances. Assuming that each element is of equal capacitance, the time constant for elements near the center of the structure would be longer than those near the cathode plate connection. At low frequency applications all elements are able to respond. However, as frequency increases, additive resistances to elements deeper within the structure create a situation in which the RC time constant begins to prohibit a response to

the higher frequencies. Increasing the frequency further effectively eliminates capacitive elements from the circuit moving from those deep within the pellet out to those near the silver-coated cathode contact. This effect is known as capacitance roll-off and is one of the most prevalent ways to observe the negative effects of ESR in these devices [6].

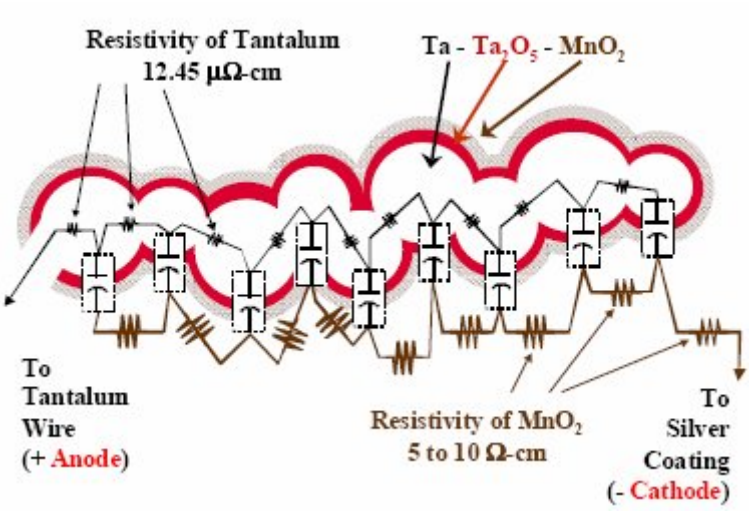

Fig 3.9 Distributed capacitive elements within the tantalum pellet structure [4].

3.5 Conclusion

The history of tantalum capacitors discussed in this chapter illustrates how their construction has evolved over time, allowing them to be implemented in a wide array of applications. With this evolution, the physical construction of these capacitors has not changed drastically from one generation to the next. While solid tantalum capacitors are fairly established in today's market, the reliability and electrical issues associated with them are becoming more significant as the technologies in which they are utilized continually progress. The following chapter will discuss the next step in evolution for solid tantalum capacitors, in which both reliability and electrical performance will

improve with a cathode material change from MnO_2 to an inherently conducting polymer (ICP).

CHAPTER FOUR

MODERN TANTALUM CAPACITORS

4.1 Modern ICP Cathode

While solid tantalum capacitors perform very well, they need to be constantly improved to keep up with the demands of the technologies in which they are used. Some areas for improvement include increasing the surface area/volume ratio, reducing process-induced stress, eliminating ignition, increasing conductivity, lowering ESR, and improving capacitance roll-off.

The consensus among most capacitor manufacturers seems to be that changing the cathode material to an ICP will improve the majority of these areas dramatically. In the area of reliability, the use of polymers will reduce process-induced stress failures. While MnO_2 is a rigid crystalline material, polymers are flexible materials that can be applied into small channels and holes without causing damage to the dielectric. Eliminating MnO_2 also removes an abundant source of oxygen used in fueling ignition failures. Based only on the reduction of stress failures and reduction of ignition, the use of ICPs shows great promise for improved reliability.

While an improvement in reliability is a huge benefit, the new materials must also provide improved electrical performance. An ICP, or inherently conducting polymer, is an organic polymer that possesses the electrical properties of a metal while retaining the mechanical properties of a conventional polymer [13]. One of the key properties of an ICP, in conduction, is conjugated double bonds along the backbone of the polymer chain. In conjugation, bonds alternate between single and double. Every bond contains a

localized sigma (σ) bond which is a strong chemical bond. In addition, every double bond also contains a weaker pi (π) bond. While the σ bonds are localized and immobile, the π bonds are less localized and more associated with the entire polymer chain. The delocalized π bonds thus create a path for charge movement along the polymer chain. However, conjugation alone is not enough to make a polymer conductive. The second key property in ICP conduction is doping. In order to be conductive, the polymer must have an electron removed or inserted to allow for the flow of free carriers. This local addition or subtraction of an electron creates a radical cation, known as a polaron, which serves as the mobile charge along the polymer chain [14].

By controlling the doping level of the polymer, conductivity ranging from highly insulating to highly conducting can be achieved as illustrated in Fig 4.1. Depending on how the doping is achieved, the polymer can also be made as either a p-type or n-type material [13]. In the case of the KEMET capacitors, p-type semiconducting PEDOT is used. When the polymer is conjugated it contains delocalized π bonds along the polymer chain, and the material is also doped p-type using an anion dopant [15].

The ability to control the level of conductivity in ICPs provides a significant electrical benefit over MnO_2. This advantage becomes clear when examining the resistive elements of the RC-Ladder effect. Higher conductance means lower resistance, which in turn reduces the time constants for all capacitive elements. These lower time constants allow a better response at higher frequencies, thus reducing the overall RC-Ladder effect and increasing operational frequency of the device [11].

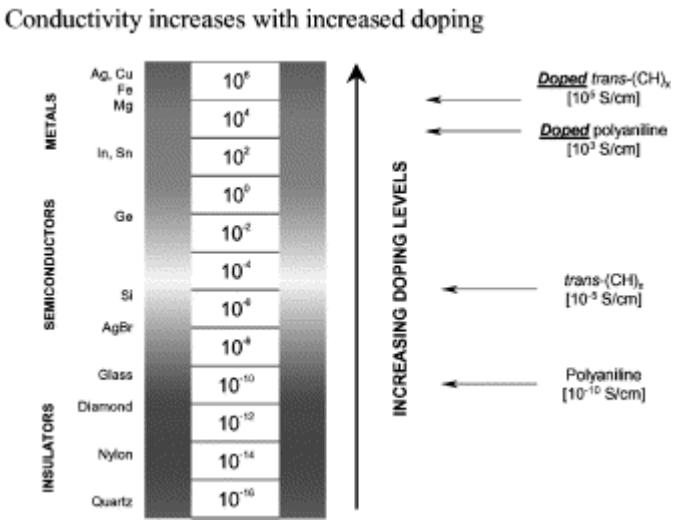

Fig 4.1 Conductivity of electronic polymers [13].

The self-healing properties of MnO_2 contributed significantly to making solid tantalum capacitors practical from the beginning. Self-healing has also been observed to take place in capacitors with ICP cathodes. There are two possible scenarios that result in a self-healing process in polymer cathodes. The first possibility is that an increase in oxygen levels causes a higher resistivity in the polymer, in a very similar fashion to the lower oxide states of MnO_2. The second possibility is that in an evaporation process, heat causes the polymer to vacate the affected area [9].

The first mechanism is theorized to occur by a changing oxygen level in the polymer. It is thought to begin with the heating of both the Ta_2O_5 dielectric as well as the polymer near the fault site. As the dielectric heats, it releases oxygen which is then absorbed by the heated polymer. The increase in oxygen content results in an increased resistivity of the polymer, essentially halting any further conduction at the site, in much the same manner as oxygen depletion from MnO_2 increases its resistivity [9,16].

The second mechanism is theorized to occur based on the vaporization temperature of the ICP. It is thought that localized heating at the fault site could raise the temperature of the polymer beyond the vaporization point, thus vacating the site and preventing conduction. This mechanism is illustrated in Fig 4.2. Sites with significant leakage current, caused by dielectric cracks or impurities such as nickel, can locally heat the polymer enough to evaporate it over time. This process does not eliminate the fault site itself, but leaves an open connection to it, effectively eliminating it from the capacitor structure [11,16].

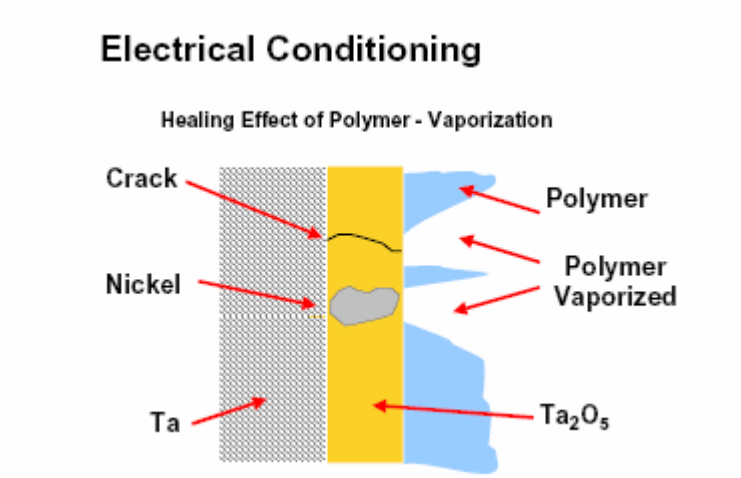

Fig 4.2 Polymer self-healing by vaporization [9].

Regardless of which theory models the actual mechanism best, there is some sort of fault correction occurring, making ICPs a possible replacement for MnO_2. As an added bonus, the polymer can be deposited in a dip and dry process very similar to that used to deposit MnO_2 in established processes. With the similarities in self-healing and manufacturing processes, as well as the reliability and electrical benefits associated with

a polymer cathode, the change from MnO_2 to an ICP provides significant improvements without a significant change to overall processes [9,11,16].

4.2 Future Trends

Today solid tantalum capacitors hold a major market share in the capacitor industry. While they are currently the best option when considering volumetric efficiency, further powder developments will be necessary to maintain and extend this advantage. A major case for moving away from tantalum capacitors stems from the material itself. Tantalum is a relatively rare ore in terms of its abundance on earth. While there are still significant amounts able to last for many years, the locations in which the ore is mined pose problems. Many of the largest suppliers of mining and refining tantalum ore are located in war-torn regions, such as the Congo, resulting in a situation analogous to African conflict diamonds. For ethical reasons, capacitor manufacturers obtain tantalum from the remaining suppliers outside of these regions. Restrictions like these lead to increased costs across the board. Alternatives to tantalum include niobium and ceramic materials [17].

From the perspective of the periodic table, niobium is a viable alternative for tantalum. Comparatively, niobium is more abundant, has a higher dielectric constant, and is cheaper and less restrictive to obtain. The main problem when considering niobium as an alternate solution is that it requires a higher dielectric thickness to match the current level of reliability maintained with tantalum capacitors, thus negating the benefits associated with the higher dielectric constant. An additional problem is that niobium must be heavily refined before it is useful. The refineries that produce capacitor-grade

niobium are coincidentally the same refineries that produce tantalum. Going through the same middle-man essentially eliminates all cost benefits associated with niobium. Until the cost of niobium offers a significant advantage over tantalum there will not be a serious push to develop the material from a reliability and performance standpoint. For the time being, penetration into tantalum-dominated markets will remain minimal [17].

Certain classes of capacitors use ceramic materials for the dielectric layer. While solid tantalum capacitors rely on the tantalum pellet for increased surface area, ceramic capacitors use a layered construction of alternating metal and ceramic materials. Ceramic capacitors have made enormous strides in the area of volumetric efficiency in recent years. Within the past decade, the volumetric efficiency ratio of tantalum to ceramic capacitors has reduced from approximately 100:1 to nearly 3:1. Large advances in thinning ceramic dielectrics have also been made, increasing the capacitance per layer as well as the overall number of layers within a given package. While the continuation of capacitance gains in ceramic materials may require the conversion from a thick film to a thin film process, the progress seen already is causing many manufacturers to switch from solid tantalum to ceramic capacitors [17,18].

In order for tantalum capacitors to keep pace with the growth of the technologies in which they are used, they need to be constantly improved. The mutual consensus among capacitor manufacturers seems to be that the inherently conducting polymer cathode is a necessary improvement. There are many possibilities for the type of ICP used in capacitors, including well-known materials such as PEDOT, Polyaniline, and Polyacetylene. Much research and development is currently taking place in order to

optimize the use of ICPs in manufacturing processes, and significant improvements over MnO_2 are already being observed. These benefits deal mostly with the increase in conductivity and the large reduction in ignition failures. While tantalum capacitor manufacturers are making every stride to stay competitive, niobium and ceramic capacitors are also emerging as possible competitors and possibly even replacements. There is a bit of uncertainty as to which type of capacitor will dominate the market share in the years to come; however, it is certain that this decision will be made based on measures of cost and performance.

4.3 MIS Theory

Solid tantalum capacitors are very complex systems when considering their associated materials and geometric structure. Developing a better understanding of these devices and how they function is a key component in continually improving their performance. One way to help accomplish this is to investigate them in new ways. While we learned about the complex construction of these devices in Chapter 3, the basic structure of modern tantalum capacitors can still be represented schematically as illustrated in Fig 4.3. From a geometric standpoint, this representation is very simplistic; however, when looking at the materials, it has an appropriate capacitor structure. This structure looks, not surprisingly, like the parallel plate capacitor model described by Equation (2.1), with a tantalum anode, PEDOT cathode, and Ta_2O_5 as the dielectric. However, there is one exception: the ICP PEDOT is doped to a semiconducting level of conductivity for these devices. Therefore, instead of being represented by a metal-insulator-metal (MIM) structure, as is commonly thought for discrete devices, solid

tantalum capacitors are actually represented by a metal-insulator-semiconductor (MIS) structure. This structure is relatively unknown by capacitor manufacturers.

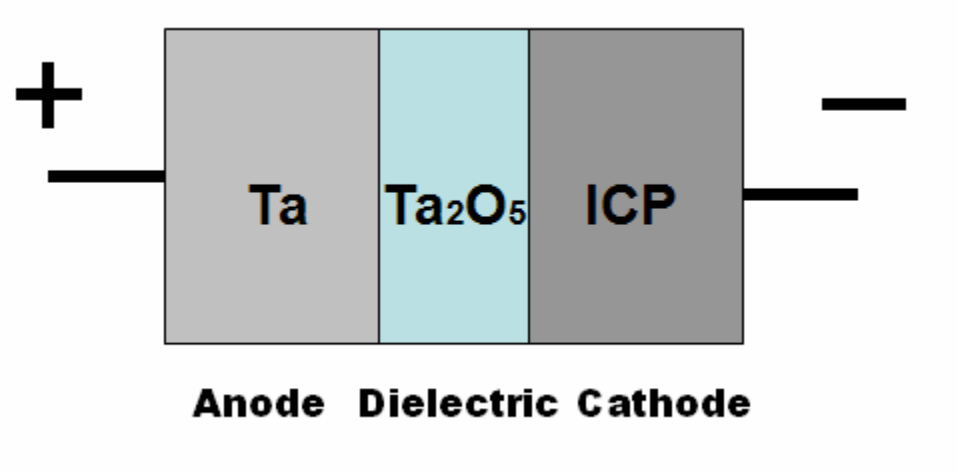

Fig 4.3 Basic Structure of modern Ta capacitors.

However, if the cathode material is based on an inorganic semiconductor, such as the one illustrated in Fig 4.4, it becomes an MIS capacitor that is very well characterized and understood in modern microelectronics.

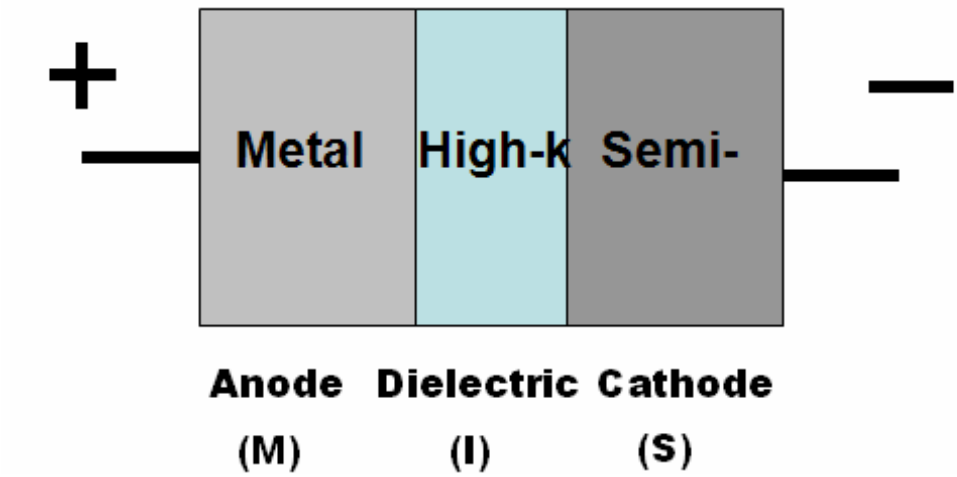

Fig 4.4 Basic MIS device structure.

By drawing this comparison, it is now reasonable to assume that solid tantalum capacitors can be measured and characterized in a manner similar to MIS devices. Before we can delve any further into this relatively radical view, we must first review the structure on which this assumption is made, the MIS capacitor.

In its simplest form, the MIS capacitor is a planar structure made up of layers of material. The base layer, and overall structural support, is an inorganic semiconductor. Most commonly this material is silicon and is doped either p-type or n-type, depending on the application, and serves as the cathode connecting material. An Ohmic contact must be made to the back end of this layer to serve as the actual cathode plate. On top of the semiconductor, a layer of oxide is thermally grown to create the dielectric layer. A metal layer, often high-conductivity polycrystalline silicon, is deposited on top of the oxide to create the anode plate and contact. Unlike tantalum capacitors, which are discrete devices, MIS capacitors can have numerous devices built on a single semiconductor substrate. This planar structure is illustrated in Fig 4.5 [19,20].

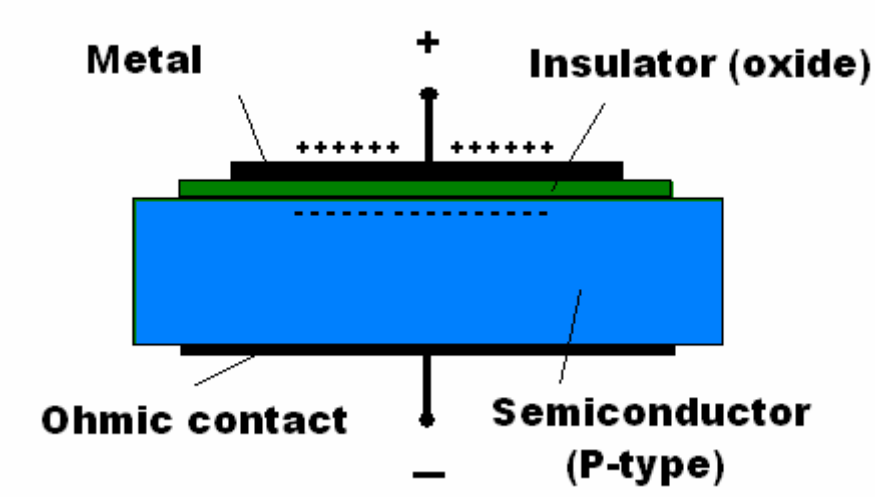

Fig 4.5 Planar structure of an MIS capacitor.

The functionality of an MIS device as a capacitor can be easily explained by comparing it to a traditional parallel plate capacitor. In a parallel plate structure, when a negative bias is applied to the anode a sheet of negative charge exists along the anode plate, a sheet of positive charge exists along the cathode plate, and an electric field is induced between the two. The capacitance for this structure is given by Equation (2.1). If the cathode plate of this structure is replaced with a p-type semiconductor substrate we get the MIS capacitor illustrated in Fig 4.5. By applying a negative bias to the anode again, we get negative charges along this plate, and an electric field is induced across the dielectric layer. If this electric field is strong enough to penetrate into the semiconductor substrate, the majority carrier holes would experience a force moving them towards the semiconductor-oxide interface. This accumulation of charge, on the cathode side of the oxide, acts as the cathode "plate," much like the parallel plate example. If the polarity of the applied bias were reversed, a positive charge would exist on the anode plate and the induced electric field would be in the opposite direction. In this case, if the field penetrates into the semiconductor substrate, the majority carrier holes would experience a force pushing them away from the semiconductor-oxide interface. As holes are pushed away, a negative space-charge region, known as the depletion region, is created due to fixed ionized acceptor atoms. This space-charge region moves the cathode "plate" away from the interface by a depletion width x_d, illustrated in Fig 4.6, thus changing the effective dielectric thickness and the overall capacitance of the structure [19,20].

This bias dependent capacitance is what differentiates MIS from MIM capacitors, as well as leads to the various modes of operation of MIS devices. The modes of

operation include Flatband, Accumulation, Depletion, and Inversion. Each mode displays unique characteristics determined by the complex charge distribution associated with the depletion width, and in turn, the applied bias. The details of these modes of operation will be further discussed in the following sections.

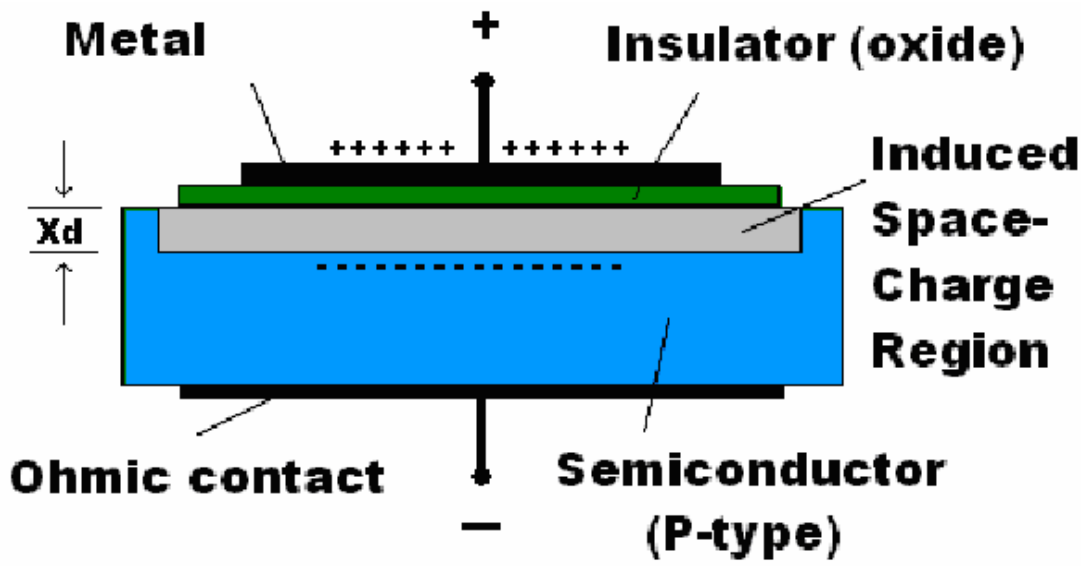

Fig 4.6 Induced space-charge region.

In order to examine the modes of operation of an MIS capacitor we must first consider its band diagrams. Fig 4.7 illustrates the separated components of an MIS band diagram. This particular system consists of aluminum as a metal, p-type silicon as the semiconductor, and SiO_2 as the insulator. Notice that the work function of the aluminum (Φ_M) is less than the work function of p-type silicon (Φ_S). The differences in the metal and semiconductor work functions cause a transfer of electron charge from metal to semiconductor when these components are brought into intimate contact. Without an external bias, this charge transfer will occur until the Fermi level (E_f) is constant through all the materials and the system is in equilibrium.

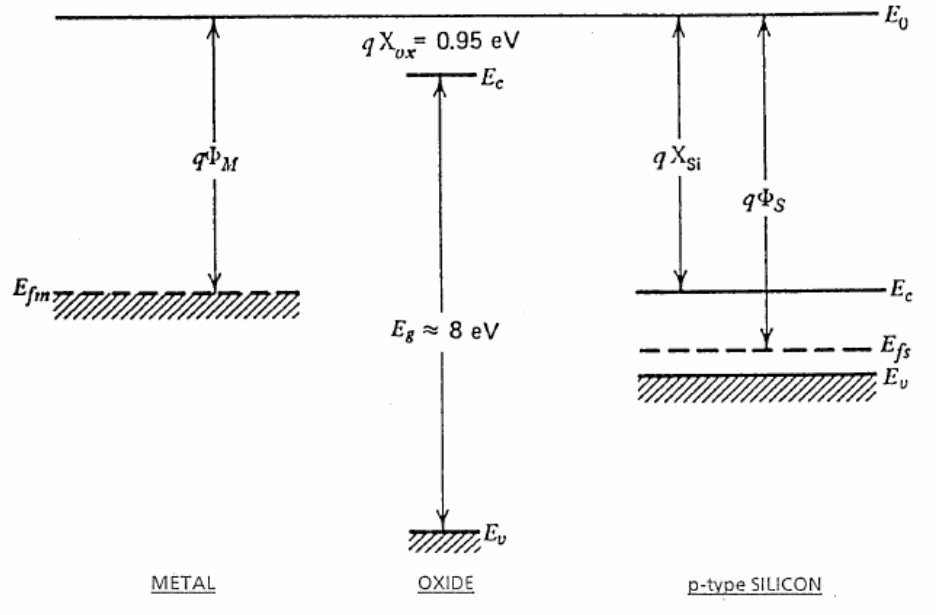

Fig 4.7 Separated band diagram [19,20].

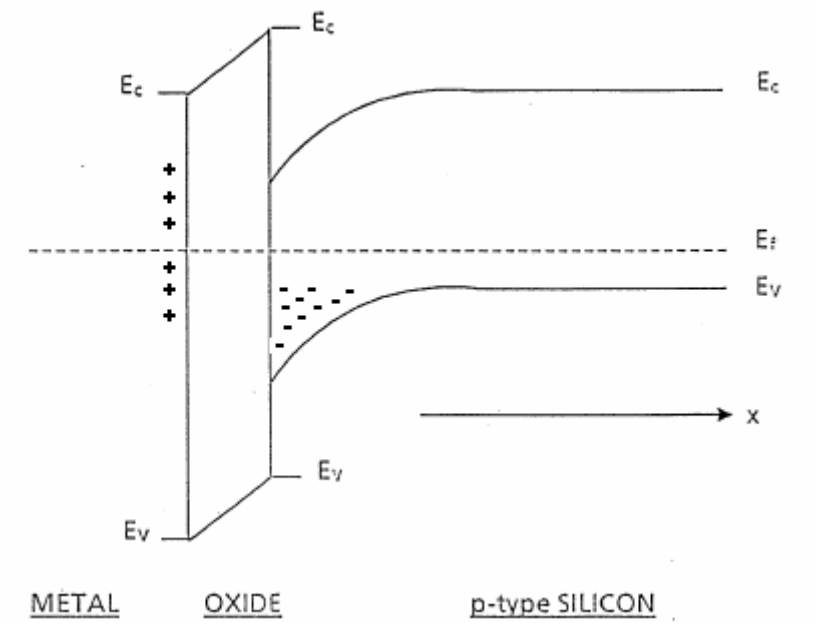

Fig 4.8 Equilibrium band diagram [19,20].

The results, illustrated in Fig 4.8, are a sheet of positive charge on the metal surface, a space-charge region of ionized acceptors in the silicon, and the bending of the bands to keep the Fermi level constant [19,20].

4.3.1 Flatband

The first mode of operation in MIS devices that we will discuss is the Flatband mode. This mode is called Flatband because it occurs when all of the bands across the device are flat. Looking again at the equilibrium band diagram in Fig 4.8, we can see that the Fermi level through the device is constant. However, the energy bands are not constant due to the built-in voltage which is caused by the inherent work function difference between the metal and the semiconductor. In order to bring the device into Flatband mode, a bias must be applied to exactly compensate for this difference. This bias is known as the Flatband Voltage, and its ideal case is given as,

$$V_{FB} = \Phi_M - \Phi_S = \Phi_{MS} \tag{4.1}$$

where V_{FB} is the ideal Flatband voltage, Φ_M is the metal work function, Φ_S is the semiconductor work function, and Φ_{MS} is the metal-semiconductor work function difference. Since the semiconductor is p-type silicon, the Flatband Voltage is negative with respect to the substrate. When the Flatband Voltage is applied, it exactly compensates for the metal-semiconductor work function difference resulting in the Flatband mode illustrated in Fig 4.9. This mode cancels all of the charge stored in the semiconductor [19,20,21].

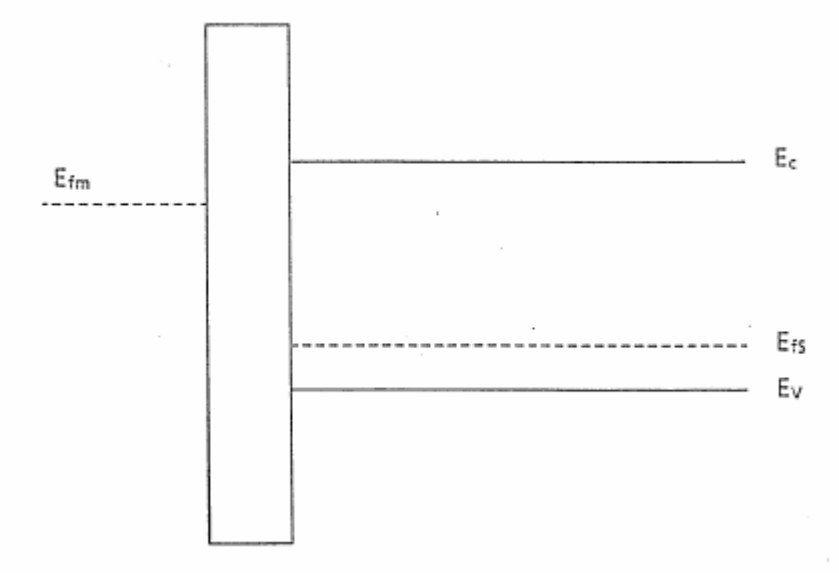

Fig 4.9 Flatband band diagram [19,20].

4.3.2 Accumulation

If a bias is applied to the metal that is more negative than V_{FB}, excess holes are attracted to the Si/SiO_2 interface, producing an accumulation layer of holes near the surface. This is known as the Accumulation mode, and, as illustrated in Fig 4.10, the bands bend up near the Si/SiO_2 interface because the surface is more p-type than the bulk under this bias mode. In this mode the capacitance of the system behaves like that of a parallel plate capacitor between the metal and the accumulation layer, and thus the capacitance of the MIS system can be written as,

$$C = \frac{\kappa_{SiO_2} \times \varepsilon_0}{t_{OX}} A = C_{OX} \tag{4.2}$$

where C is the overall capacitance of the system, κ_{SiO2} is the dielectric constant of SiO_2, ε_0 is the permittivity of free space, t_{OX} is the dielectric thickness, and A is the area of the

capacitor plates. This capacitance is known as the oxide capacitance (C_{OX}), because it is due to charge stored on either side of the oxide [19,20,22].

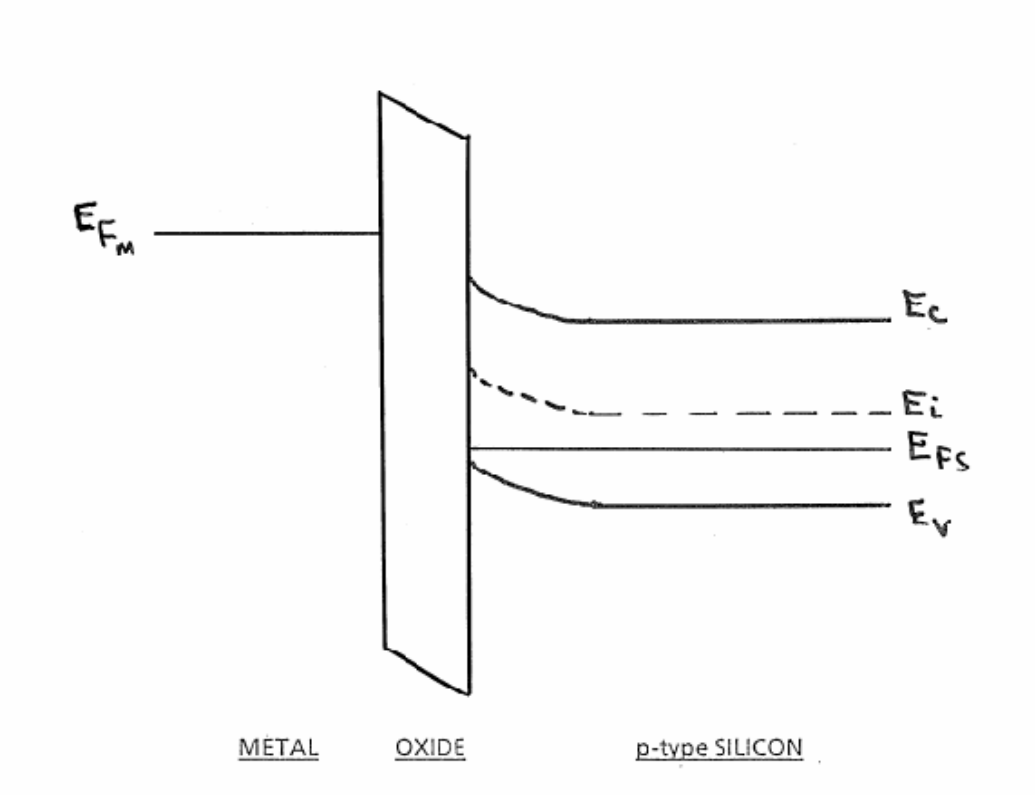

Fig 4.10 Accumulation band diagram [19,20].

4.3.3 Depletion

For biases that range from less negative than V_{FB} to slightly positive, the MIS capacitor is in the Depletion mode. This is also the mode that the device was in at equilibrium in Fig 4.8. Since the bias is less negative than V_{FB}, mobile holes at the Si/SiO_2 interface are repelled away from the surface. The region out of which these mobile carriers are pushed is the depletion region. The band diagram for the MIS system in Depletion mode is shown in Fig 4.11. The bands are shown to bend down at the

surface since it is depleted and is much less p-type than the bulk. However, the concentration of holes is still greater than the intrinsic carrier concentration (n_i). The depletion region extends into the bulk a certain distance known as the depletion width, x_d, and can be written as [19,20,22],

$$x_d = \sqrt{\frac{2\varepsilon_{Si}\Psi_S}{qN_a}} \tag{4.3}$$

where ε_{si} is the permittivity of the semiconductor, q is the electronic charge, N_a is the semiconductor doping concentration, and Ψs is the total band bending. By examining Equation (4.3) we can make a few observations as to how the depletion width will be affected by different parameters. As would be expected, x_d is affected by the external applied bias. As the bias increases, Ψs also increases, leading to an increase in x_d. The depletion width is also affected by the semiconductor doping concentration. As the doping concentration increases, there are more carriers that must be pushed away from the interface to form the depletion region. Therefore, an increase in N_a results in a decrease in x_d at a given bias [19,20].

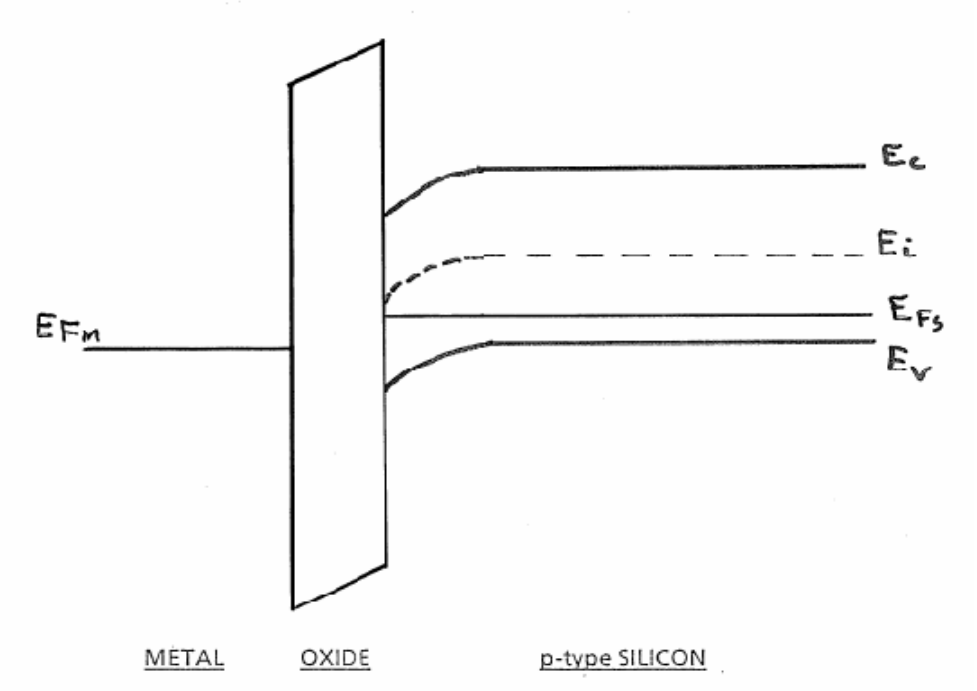

Fig 4.11 Depletion band diagram [19,20].

In depletion there is no longer an accumulation layer at the surface, so the system no longer behaves exactly like a single parallel plate capacitor as given in Equation (4.2). Instead there is a capacitance due to the oxide, C_{OX}, as well as a capacitance due to the depletion region, C_D. The total MIS system now behaves like the series combination of these two capacitors as illustrated in Fig 4.12. The capacitance of the depletion region can be written as,

$$C_D = \frac{\varepsilon_{Si}}{x_d} A \tag{4.4}$$

because the depletion region separates the "plate" at the semiconductor-oxide interface from the "plate" at the edge of the depletion region. The semiconductor in the depletion

region acts as a dielectric with a thickness x_d because the surface is depleted of mobile carriers and therefore highly insulating. Much like the parallel plate model from Equation (2.1), C_D is inversely related to the depletion width. The series combination of C_{OX} and C_D yields the total capacitance, C_T, of the MIS system in Depletion mode and can be written as,

$$C_T = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_D}} = \frac{C_D C_{OX}}{C_D + C_{OX}} \tag{4.5}$$

Thus, according to Equation (4.5), C_T decreases as C_D decreases in Depletion mode, which happens when x_d increases. Therefore, C_T decreases with an increase in applied bias [19,20,22,23].

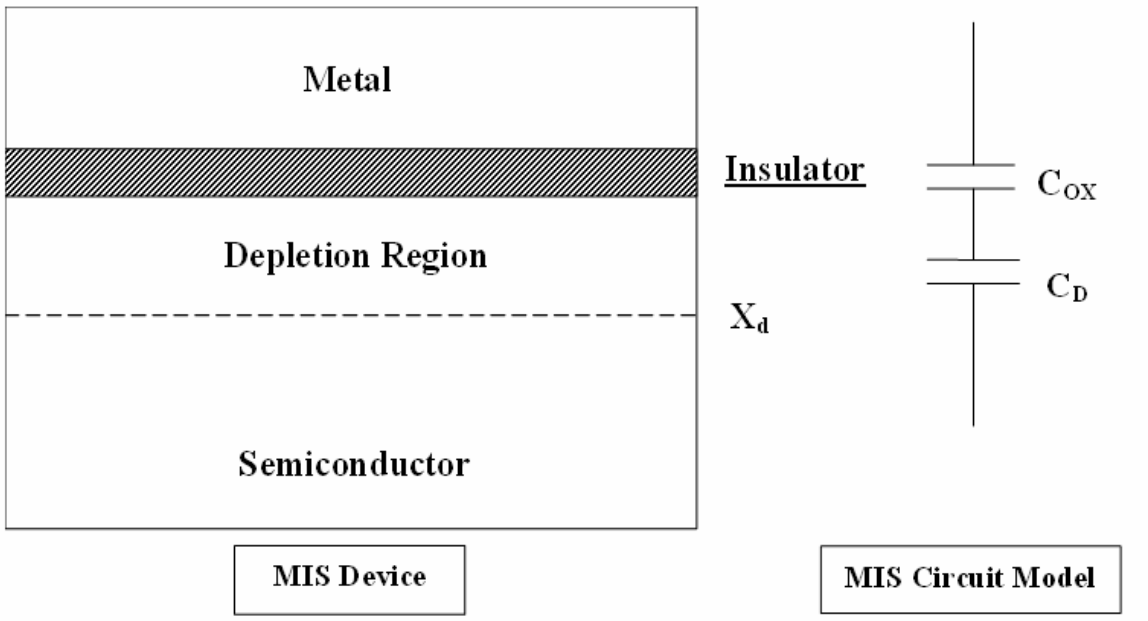

Fig 4.12 MIS device and circuit model in Depletion mode.

4.3.4 Inversion

When a relatively large positive bias is applied to the MIS system, the hole concentration near the surface decreases while the electron concentration increases. When the intrinsic level, E_i, drops below the Fermi level, E_F, near the interface, the surface has inverted from p-type to slightly n-type. Once this occurs the surface is considered to be in weak inversion. When the device is in Depletion mode it has only immobile ionized acceptor atoms near the surface. Once the device enters into Inversion mode, it also has an inversion layer of mobile electrons. This layer is very similar to the accumulation layer previously discussed; however, it is an "accumulation" of minority carrier electrons caused by thermal generation. Therefore, the surface concentration of the semiconductor is inverted when compared to the bulk.

As the bias is increased, the electron concentration at the surface continues to increase. Once the surface potential, $q\Phi_S$, is equal in magnitude to the bulk potential, $q\Phi_B$, the surface is at the onset of strong inversion, meaning that the minority carrier surface concentration is now equal to the majority carrier bulk concentration. Strong inversion is generally the condition referred to when discussing the Inversion mode. With the Si/SiO_2 interface now fully inverted, the MIS system has two conducting electrodes, the metal and the inversion layer. When looking at the charge distribution of the device in Inversion mode, there is still the fixed charge of the depletion layer; however, now that mobile minority carriers have been generated, there is an inversion layer at the surface. As long as the inversion layer has been generated at the surface, there is no longer a depletion capacitance as in Fig 4.12. Instead there are layers of

charge on either side of the oxide much like in Accumulation mode. The MIS capacitor again behaves like a parallel plate capacitor with a capacitance equal to C_{OX} Equation (4.2). An Inversion mode band diagram is illustrated in Fig 4.13 where $q\Psi_S$ is the total band bending, $q\Phi_S$ is the surface potential, $q\Phi(x)$ is the semiconductor potential, and $q\Phi_B$ is the bulk potential [19,20,22].

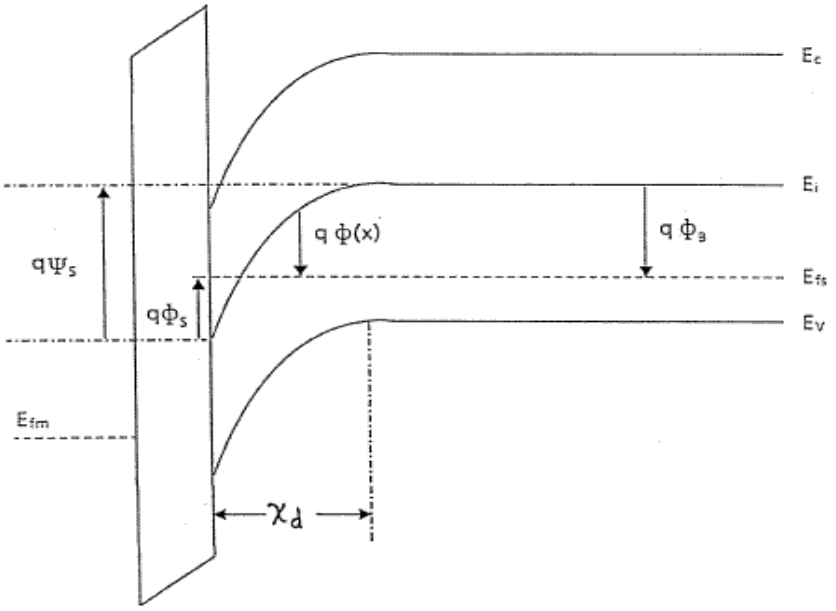

Fig 4.13 Inversion band diagram [19,20].

4.3.5 Capacitance-Voltage Curves

The modes of operation just discussed show that the capacitance of an MIS system is dependent on the applied bias. In Fig 4.14 a graphical representation of this dependence is illustrated on a Capacitance-Voltage or C-V curve. A C-V curve is composed of two separate measurements, one made at a high frequency and one at a low frequency. To make these measurements, a dc bias is slowly ramped from negative to positive values, and a small ac signal is superimposed on to this bias. The small ac signal

is used to measure the capacitance of the device at various dc biases. This method of performing a C-V measurement is consistent with how C-V curves are created from traditional MIS devices. Next we will discuss why the curve appears as it does in the low frequency and high frequency measurements [19,20,22].

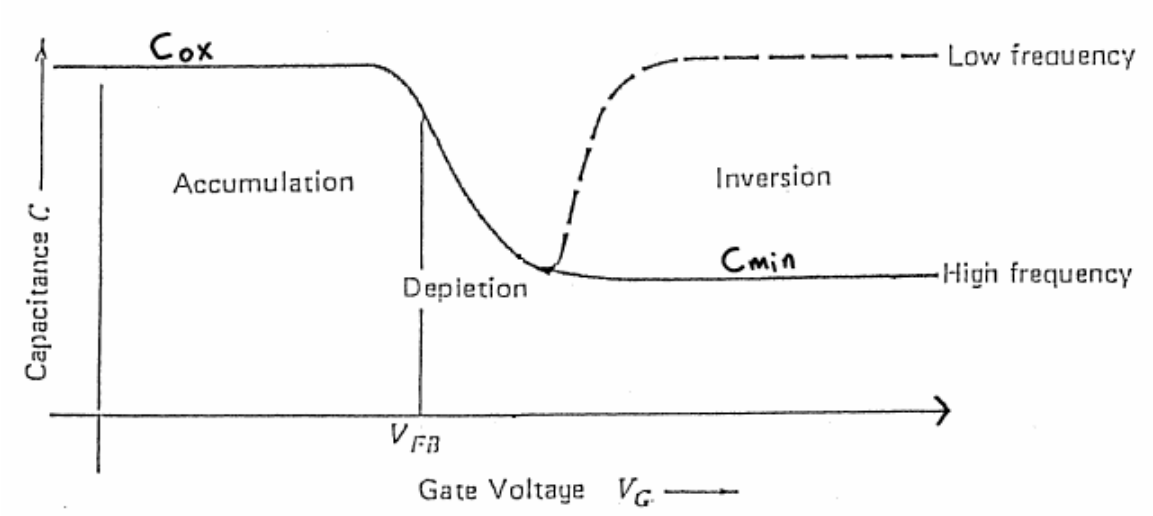

Fig 4.14 C-V Curve of MIS capacitor with a p-type substrate [19,20].

The first measurement is that of a low frequency or quasi-static ac signal. When the bias is very negative the curve shows that the system is in the Accumulation mode. As described by Equation (4.2), the system behaves like a parallel plate capacitor and has a constant capacitance, C_{OX}. When the bias is increased further, the surface starts to become depleted, and the variations of the applied bias induce variations in the depletion charge. The overall capacitance is now determined by the series combination of C_{OX} and C_D as illustrated in Fig 4.12. As the device moves further into the Depletion mode the depletion width increases, thus decreasing C_D and the overall capacitance. As the bias is further increased, an inversion layer begins to form. The variations in bias now bring

about variations in the inversion charge, eventually bringing the system back to a parallel plate model with capacitance C_{OX}.

The second measurement uses a high frequency ac signal, typically 1MHz in traditional MIS devices. In making a high frequency C-V measurement, the portions of the curve in which the device is in accumulation and depletion are identical to their counterparts in the low frequency measurement. However, the minority carriers that populate the inversion layer are generated thermally, which is a relatively slow process at room temperature. Therefore, when using a high frequency signal, thermal generation cannot generate minority carriers fast enough to support the variation of charge within the inversion layer. The variation of charge with the variation of applied bias is no longer supported by the inversion charge, but now by the depletion charge. In the high frequency measurement, at high biases, the depletion layer supports the variation of charge that gives rise to the measured capacitance, and the overall capacitance remains a series combination of C_{OX} and C_D. As the capacitance on the C-V curve decreases, it eventually reaches a minimum value that corresponds with a maximum depletion width, x_{dmax}, which can be written as,

$$x_{d\max} = \sqrt{\frac{4\varepsilon_{Si}\left|\Phi_B\right|}{qN_a}} \tag{4.6}$$

Therefore, the depletion width of the device reaches a maximum value when the total band bending is equal to twice the bulk potential, a condition known as the onset of strong inversion [19,20,22,23,24].

4.4 Tantalum MIS Devices

Tantalum capacitors are rarely studied outside the capacitor industry; however, material components of these capacitors are often researched in other fields. Ta_2O_5 has recently gained attention in the semiconductor industry as part of a search for acceptable high-k dielectric materials. Of the possible high-k dielectrics, Ta_2O_5 is very attractive because it has a relatively high dielectric constant of about 27, it can be deposited in thin film form, and it is an IC-compatible material [25].

The main way in which Ta_2O_5 has been studied is as part of a parallel plate or MIM (metal-insulator-metal) system. These MIM capacitors typically consist of an amorphous layer of Ta_2O_5 deposited by MOCVD (Metallo-Organic Chemical Vapor Deposition) and PVD-deposited (Physical Vapor Deposition) TiN electrodes [26,27]. These studies identified Ta_2O_5 leakage current as being composed of several mechanisms: a polarization current attributed to dielectric relaxation [26], a conduction current attributed to Poole-Frenkel mechanisms [27,28], and a resistance degradation attributed to ionic diffusion that agrees with Space-Charge Limited theory [26,27].

Ta_2O_5 has also been studied in planar MIS forms as a candidate for storage capacitors in DRAMs. The structures used were much like the MIM studies above but replaced the cathode with a silicon-based electrode ($TiN/Ta_2O_5/SiN/Si$). The leakage current mechanisms observed showed the device to be polar as expected. In forward bias operation, with a positive bias applied to the anode, the current was shown to be Poole-Frenkel assisted by Fowler-Nordheim Tunneling from the bottom Si electrode. In reverse

bias operation the current was also Poole-Frenkel but assisted by Schottky injection from the TiN electrode [29]. These mechanisms are summarized in Fig 4.15.

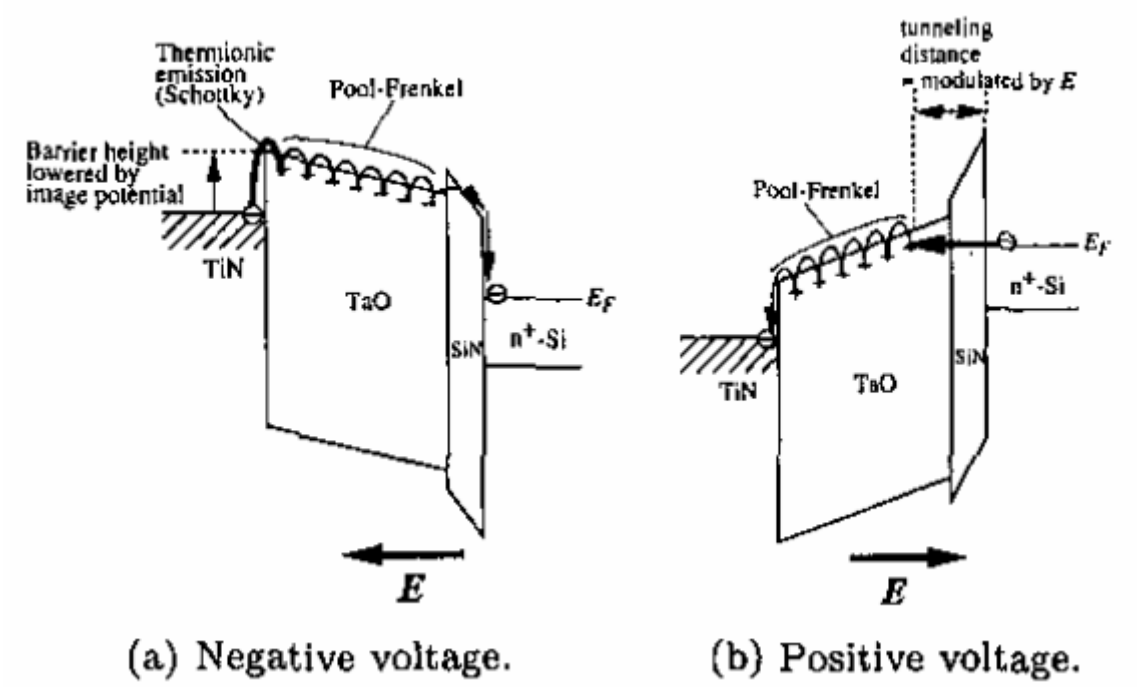

Fig 4.15 Leakage current mechanisms of TiN/Ta_2O_5/SiN/Si capacitors [29].

While these studies of Ta_2O_5 in MIM and MIS devices show a great insight into the leakage current mechanisms of the dielectric, they are still very simplistic structures when compared to packaged tantalum capacitors. A study of packaged capacitors with MnO_2 cathodes reveals low-field conduction mechanisms of ionic conduction and Space-Charge-Limited current flow [30]. Another study on similar parts shows conduction in forward bias operation of Poole-Frenkel and Schottky mechanisms. The same study also examined a type of ICP capacitor and found conduction mechanisms of Poole-Frenkel overlapped with Space-Charge-Limited current injection [31].

4.5 Conclusion

In this chapter we discussed modern tantalum capacitors that had their MnO_2 cathode replaced with a semiconducting polymer. By looking at a basic representation of the structure of these capacitors, we conclude that they can be classified as MIS systems. The capacitors that will be investigated as part of this thesis were manufactured by KEMET Corporation and use p-type PEDOT for the cathode material. In order to characterize these devices, we will investigate their capacitance to show that while they are discrete devices, they exhibit voltage dependencies similar to IC MIS devices. In addition, we will also investigate current-voltage characteristics in order to identify the dominant leakage mechanisms. In the next chapter we will discuss in more detail the conduction mechanisms previously mentioned that could contribute to the overall leakage current in modern tantalum capacitors.

CHAPTER FIVE

CONDUCTION MECHANISMS

The brief literature review in Chapter 4 revealed several possible conduction mechanisms for Ta_2O_5 in MIM and MIS systems as well as packaged tantalum capacitors. In order to better understand tantalum capacitors as MIS systems, these conduction mechanisms must first be fully understood. While a large variety of mechanisms were mentioned in the literature review, the following sections will focus on the more dominating and frequently mentioned mechanisms: specifically the Poole-Frenkel Effect, Space-Charge-Limited Current, Fowler-Nordheim Tunneling, and the Schottky Effect.

5.1 The Poole-Frenkel Effect

The Poole-Frenkel Effect is a bulk-limited conduction mechanism that is often used to explain conduction in thin dielectric films. The Poole-Frenkel (PF) Effect is a thermal emission of charge carriers from Coulombic traps in the bulk of a dielectric or semiconductor, enhanced by the application of an external electric field [32]. In order for traps to experience the PF Effect they must be neutral when filled and charged when empty. Traps that are neutral when empty do not experience the effect due to a lack of Coulombic potential [33]. The PF mechanism is driven by the applied electric field. The field reduces the barrier height on one side of the trap and in turn increases the probability that an electron will escape from the trap. This process is illustrated in Fig 5.1, where a Coulombic potential well can be seen in the presence of an applied electric

field. In Fig 5.1, $q\Phi$ is the ionization potential of the trap, which is the energy necessary for an electron to escape the Coulombic attractive trap.

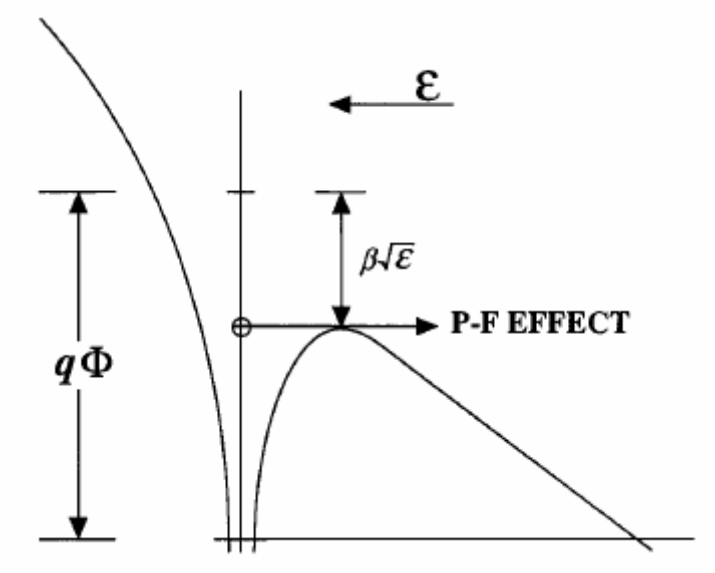

Fig 5.1 Coulombic potential well in presence of electric field [32].

$\beta\sqrt{E}$ is the amount by which the barrier is reduced by the applied electric field, E. The side of the trap that has been reduced is now at an effective ionization potential $q\Phi_{eff}$ which can be written as, [34]

$$q\Phi_{EFF} = q\Phi - \beta\sqrt{\mathrm{E}} \tag{5.1}$$

The constant, β, in the barrier height reduction is given by,

$$\beta = \sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}} \tag{5.2}$$

where ε_0 is the permittivity of free space and ε_r is the dielectric constant of the material. As we can see, β is strictly a materials parameter, meaning the barrier reduction $\beta\sqrt{E}$ is dependent on the applied field. Also, those materials with higher dielectric constants will be less sensitive to the field-induced barrier lowering.

The materials in which this effect is usually present are amorphous solids that do not have a traditional band structure [35]. Instead, when electrons escape over the effective barrier height, they enter the quasi-conduction band of the material. The quasi-conduction band and the ground state of the trap can be analogously compared to the conduction and valence bands of a crystalline solid. The conductivity due to thermal ionization of the Coulombic traps was approximated by Frenkel to be proportional to the free carrier concentration of the quasi-conduction band [36]. He also used the Boltzmann approximation and assumed that the Fermi level was located at the middle of the band gap. From these assumptions the conductivity as a function of the electric field can be written as,

$$\sigma = \sigma_0 \exp\left[\frac{\beta\sqrt{\mathrm{E}}}{2kT}\right] \tag{5.3}$$

where

$$\sigma_0 = C \exp\left[-\frac{q\Phi}{2kT}\right] \tag{5.4}$$

and C is a proportionality constant. Equations (5.3) and (5.4) make up Frenkel's first-order model of field-assisted thermal ionization of electrons from Coulombic traps which is now known as the Poole-Frenkel Effect.

By multiplying Equation (5.3) by the applied field, the current density, J, due to the PF Effect is given by,

$$J = C\mathrm{E}\exp\left[-\frac{q\Phi - \beta\sqrt{\mathrm{E}}}{2kT}\right] \tag{5.5}$$

Recall that the above equation was reached based on the Boltzmann approximation and the assumption that the Fermi level was always at mid-gap. However, the Fermi level can vary between mid-gap and ground state depending on the relative acceptor concentration [32]. Considering this, a more general expression for PF current density is given by,

$$J = C\mathrm{E}\exp\left[-\frac{q\Phi - \beta\sqrt{\mathrm{E}}}{\xi kT}\right] \tag{5.6}$$

where ξ is the slope parameter and varies between the limiting cases of ξ=1 and ξ=2 depending on the amount of acceptor compensation. By rearranging Equation (5.6) we can obtain the following result.

$$\ln\left(\frac{J}{\mathrm{E}}\right) = \frac{\beta}{\xi kT}\sqrt{\mathrm{E}} + \left[\ln C - \frac{q\Phi}{\xi kT}\right] \tag{5.7}$$

From Equation (5.7) we can see that a plot of ln*(J/E)* versus $\sqrt{E}$ should yield a straight line if the PF Effect dominates. This is known as a PF plot. Any region of linearity on such a plot of experimental data can be considered evidence of PF conduction. The slope of a PF plot, M, is proportional to β, and can be written as,

$$M = \frac{\beta}{\xi kT} \tag{5.8}$$

M is dependent on material and temperature and can be used as further verification of PF conduction [32].

5.2 Space-Charge-Limited Current

Space-charge is generally referred to as a space filled with a net positive or net negative charge. This phenomenon can occur in a great deal of situations associated with semiconductors and insulators. Space-charge-limited current (SCLC) conduction occurs when a contact electrode is capable of injecting either electrons into the conduction band or holes into the valence band of a semiconductor or insulator. When the initial rate of charge-carrier injection is higher than the rate of recombination, the injected carriers will form a space-charge region which will limit the current flow. Therefore, SCLC is a bulk limited process [37].

Child's Law, which gives the current density for space-charge-limited emission into a vacuum, is one of the basic equations of vacuum electronics [38]. The analog of space-charge-limited currents in a vacuum is the space-charge-limited currents in an

insulator [39]. The Mott-Gurney Law analogously predicts the current density due to SCLC in an insulator in the absence of any trapping effects and is written as, [40,41]

$$J = \frac{9}{8}\mu\varepsilon_r\varepsilon_0\frac{V^2}{L^3} \tag{5.9}$$

where μ is the free carrier mobility of the material, ε_r is the dielectric constant of the material, ε_0 is the permittivity of free space, V is the applied bias and L is the thickness of the insulator.

In single crystals trap levels are generally discrete. However, in real insulators traps are distributed in accordance with certain distribution functions and can profoundly influence the current flow [37,42]. In ideal materials with no traps, current-voltage characteristics exhibiting SCLC follow an ideal square law dependence on voltage. In materials containing some distribution of traps, the current-voltage curve can be distorted and show a much higher power dependence on voltage [39]. Modified current density equations are shown in Table 5.1 for various cases of trap distributions.

In all of the current equations of differing trap distributions, there is an underlying power law relationship between current density and voltage. The relationship is that the current density is a function of the voltage raised to a power. It is because of this relationship that evidence of SCLC can be seen by a linear region on a log-log current-voltage plot. From this type of plot, the slope of the linear region, or exponent of the power law relationship, can be used to infer the type of distribution of traps in the insulator.

Table 5.1 SCLC current density equations for varying trap distributions [37].

Trap-free	$J = \frac{9}{8}\varepsilon\mu_p \frac{V^2}{d^3}$
Traps confined in a single discrete energy level	$J = \frac{9}{8}\varepsilon\mu_p\Theta_d \frac{V^2}{d_{eff}^3}$
Traps distributed exponentially within the forbidden energy gap	$J = q^{1-l}\mu_p N_v \left(\frac{2\ell+1}{\ell+1}\right)^{l+1}\left(\frac{\ell}{\ell+1}\frac{\varepsilon}{H_b}\right)^{l}\frac{V^{l+1}}{d_{eff}^{2l+1}}$
Traps distributed in a Gaussian manner within the forbidden energy gap	$J = \frac{9}{8}\varepsilon\mu_p\Theta_d \frac{V^2}{d_{eff}^3}$ (for shallow traps) $J = q^{1-m}\mu_p N_v \left(\frac{2m+1}{m+1}\right)^{m+1}\left(\frac{m}{m+1}\frac{\varepsilon}{H_d'}\right)^{m}\frac{V^{m+1}}{d_{eff}^{2m+1}}$ (for deep traps)
Traps distributed uniformly within the forbidden energy gap	$J = 2q\mu_p N_V g_p \frac{V}{d_{eff}}\exp\left[-\frac{E_u - E_t}{kT}\right]\exp\left[\frac{2\varepsilon V}{qH_c kTd_{eff}^2}\right]$

5.3 Fowler-Nordheim Tunneling

Fowler-Nordheim Tunneling is a process by which carriers tunnel through a barrier assisted by the presence of a high electric field [24]. Due to the high electric field, carriers tunnel through a triangular barrier as opposed to the trapezoidal barrier in classical tunneling [43]. By essentially thinning the effective barrier, more carriers have a high probability of tunneling than previously with the full barrier. A qualitative representation of this process is illustrated in Fig 5.2, where Φ_B is the barrier height, x_0 is the trapezoidal barrier thickness, and x_1 is the triangular barrier thickness.

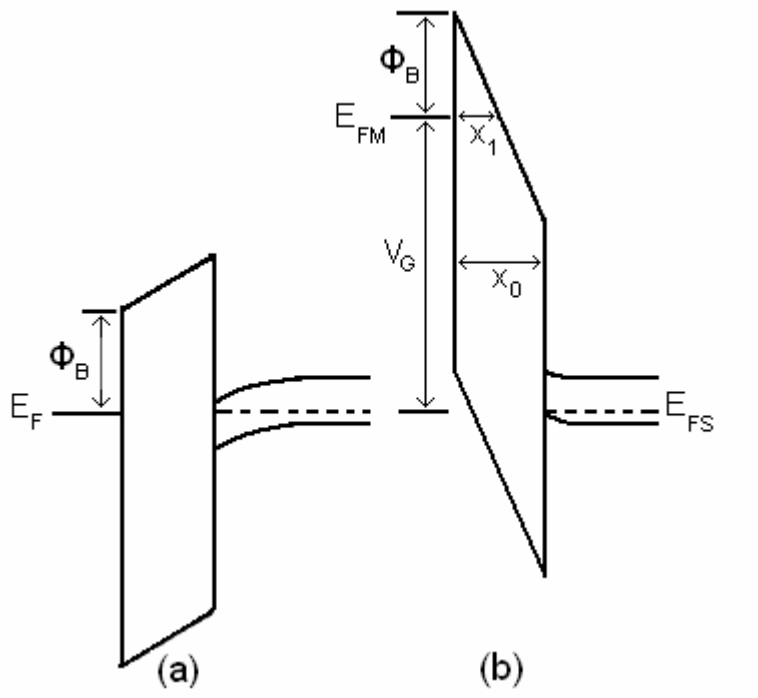

Fig 5.2 Energy band diagrams (a) no field (b) high field [44].

According to the simplest model, the current density due to Fowler-Nordheim Tunneling can be written as,

$$J = AE^2 \exp\left(-\frac{B}{E}\right) \tag{5.10}$$

where

$$A = \frac{m}{m^*}\frac{q^3}{8\pi h\phi_B} \tag{5.11}$$

$$B = \frac{8\pi}{3}\left(2\frac{m^*}{h^2}\right)^{1/2}\frac{\phi_B^{3/2}}{q} \tag{5.12}$$

and E, m, m^*, q, h, and φ_B are, respectively, the electric field, the electron mass, the effective mass of the electron in the dielectric, the electron charge, Plank's constant, and the barrier height at the injecting electrode [45].

According to Equation (5.10), a plot of $\log(J/E^2)$ versus $1/E$ should yield a linear region with a slope of B if Fowler-Nordheim Tunneling is the dominating mechanism. This type of plot is well-known as a Fowler-Nordheim or FN plot. The unknown parameters A and B in the above model can be found experimentally from an FN plot.

5.4 The Schottky Effect

The Schottky Effect is very similar to the previously mentioned Poole-Frenkel Effect. As with PF, the Schottky Effect is charge emission due to the lowering of a Coulombic barrier by an applied electric field. Instead of a fixed positive charge as in the PF Effect, the Schottky Effect depends on a mobile positive image charge created by the escaping electron. While the PF Effect is controlled by trap barriers in the bulk, the Schottky Effect is associated with interfacial barriers between a metal and a semiconductor. Therefore, the Schottky Effect is an electrode limited process. The Schottky barrier lowering due to this image charge is illustrated in Fig 5.3. The triangular barrier is reduced by the image charge and further reduced by the applied field [22,23,46].

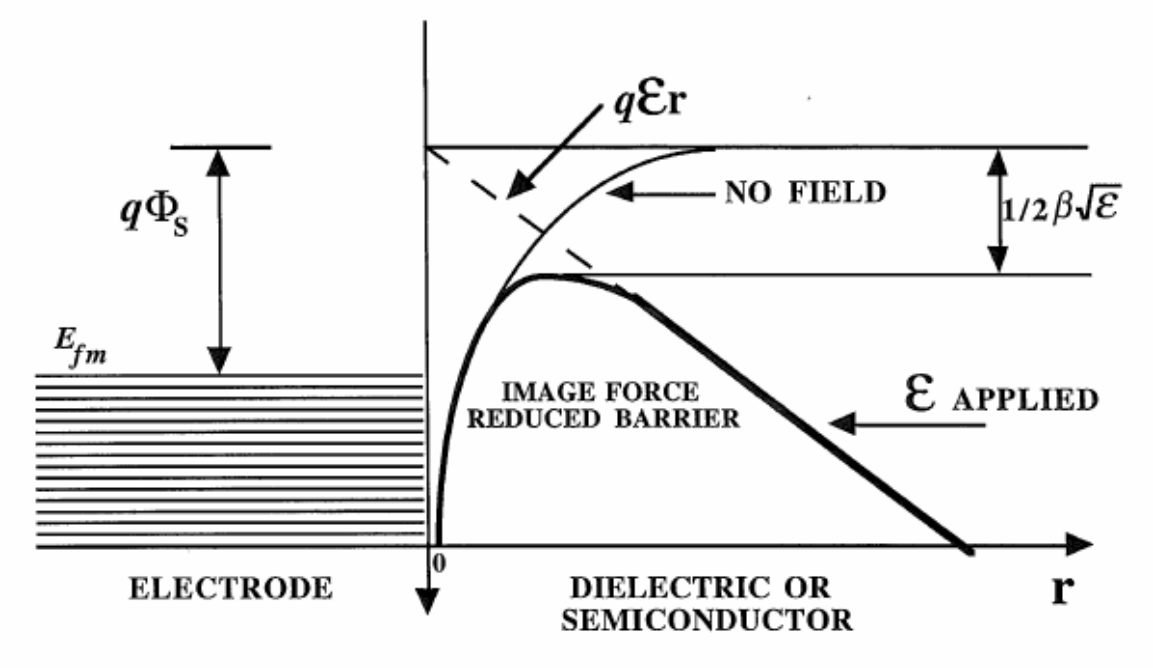

Fig 5.3 Schottky barrier lowering due to an image charge
with and without an applied field [46].

The current density due to the Schottky Effect, J_S, is given by the Richardson-Dushman equation:

$$J_S = A^* T^2 \exp\left[-\frac{q\phi_S - \frac{1}{2}\beta\sqrt{\mathrm{E}}}{kT}\right] \tag{5.13}$$

where A^* is the Richardson constant, and is given by [23]

$$A^* = \frac{4\pi e m^* k^2}{h^3} \tag{5.14}$$

By manipulating Equation (5.13) we can write:

$$\ln\left(J_S\right) = \frac{\beta}{2kT}\sqrt{E} + \left[\ln\left(A^* T^2\right) - \frac{q\phi_S}{kT}\right] \tag{5.15}$$

From Equation (5.15) we can see that a plot of ln(J_S) versus $\sqrt{E}$ will yield a straight line. This is known as a Schottky plot. A linear region on a Schottky plot is evidence that the Schottky Effect is the dominant mechanism. In very similar fashion to the PF Effect, the slope of a Schottky plot, M_S, is proportional to β and is given by,

$$M_S = \frac{\beta}{2kT} \tag{5.16}$$

The slope of a Schottky plot differs from that of a PF plot according to the amount of acceptor compensation present in the case of PF emission. M_S will differ by a factor of two when the Fermi level is near the ground state of the trap for the Poole-Frenkel Effect. However, if the Fermi level is at mid-gap there is no difference in slopes. The slope of the plot is used as a way to distinguish which mechanism is dominant [46].

5.5 Other Possible Mechanisms

The previously discussed mechanisms are not intended to be an exhaustive list of the possible leakage mechanisms that could affect the KEMET capacitors. They are, however, a very good starting point to work from according to the literature review. The literature review yielded some other secondary leakage mechanisms such as polarization current due to dielectric relaxation [26] and resistance degradation due to ionic diffusion

[26,27]. However, the Poole-Frenkel Effect, Space-Charge-Limited Current, Fowler-Nordheim Tunneling, and Schottky Effect appear to be more dominant mechanisms, especially at high fields. Therefore, these models will be the main focus when experimentally examining the leakage mechanisms of the KEMET capacitors.

CHAPTER SIX

TANTALUM CAPACITOR CHARACTERIZATION

6.1 Introduction

In previous chapters, based on the construction of tantalum capacitors as well as literature reviews of other similar devices, we made the assumption that these devices can be classified as MIS systems. In this chapter we will discuss the characterization of the modern tantalum capacitors manufactured by KEMET Electronics Corporation and show through experimental results that the MIS assumption is valid. Based on a classical approach of examining MIS devices, we will perform Capacitance-Voltage (C-V) measurements in an attempt to observe a C-V curve, such as shown in Fig. 4.14, and present evidence of the modes of operation commonly associated with an MIS device. While one of the main goals of this thesis is to show that modern tantalum capacitors are MIS systems, we must still recognize that they are in fact manufactured and intended to be used as discrete devices. In order to take this into account we must modify the parameters used and the manner in which we perform C-V measurements, while monitoring the device's capability as a discrete capacitor through nominal capacitance measurements.

We also know, from KEMET Electronics Corporation and our own measurements, that these capacitors are very polar and have an extremely limited operational range in reverse bias due to high leakage current. Therefore, in order to attempt to suppress the leakage current and increase the practical range of applied reverse bias, we will make C-V measurements at temperatures ranging from room temperature

(300K) to near liquid nitrogen temperature (100K). In addition to observing a wider range in C-V curves, conduction measurements at various temperatures will allow us to make observations on the overall temperature dependence of carrier transport in these capacitors.

The other main goal of this thesis is to identify the dominating leakage mechanisms in modern tantalum capacitors. In order to do so, we will make use of current-time (I-t) and current-voltage (I-V) measurements. I-t measurements will be used to help set up parameters for making I-V measurements. By observing the current as a function of time at a constant voltage, we can determine the RC time constant of the capacitor and decide how much of a delay is needed between measured points on the I-V curves. A secondary function of the I-t measurements is to help determine if the applied stress is damaging the devices. If the applied bias is too high for the capacitor, an I-t measurement will show an increase in current over time as opposed to a current decay. The importance of I-V curves is that they show conduction of the device under test. By plotting these curves in various ways we can determine what conduction mechanisms are present in the capacitors. We will collect I-V curves both manually and through an automatic voltage sweep. The manual measurements will be made through a progressive series of I-t measurements in order to reveal the true dc conduction at each voltage level. Theoretically this type of measurement should produce the most accurate representation of an I-V curve; however, they are incredibly time consuming and difficult to make. Therefore, we will also use an automatic voltage sweep to generate high resolution I-V curves for modeling purposes. While this type of measurement yields a certain amount

of inherent error, we will show that the information we can extract is accurate enough to qualitatively determine various leakage mechanisms.

6.2 Equipment and Procedures

6.2.1 Equipment

All C-V characteristics were collected with an Agilent E4980A Precision LCR Meter and a cryostat made by SULA Technologies. The inside of the cryostat cage contains a copper chuck used to hold the capacitors being measured. A needle-point probe holds the capacitor in place and serves as the electrical contact to the cathode while a clip wire serves as the contact to the anode. A lid covers the cage to create a vacuum seal, while an external rotary pump is used to bring the chamber to a rough vacuum. The Dewar tank of the cryostat is used to hold liquid nitrogen while an external electromagnetic pump is used to siphon the liquid nitrogen through the chamber in order to cool it. The temperature in the chamber is regulated with a LakeShore 331 temperature controller with a practical range of 100K to 400K.

All I-t and I-V characteristics were collected with an HP4156B Precision Semiconductor Parameter Analyzer and the SULA Technologies cryostat. Under normal circumstances any device being tested with the HP4156B would be measured using a Micromanipulator probe station. However, the probe station does not have the capability to cool the devices as the cryostat does. Therefore, the cryostat was connected to the device under test for all measurements. Since the cryostat was being used in a different way than it traditionally would be, we conducted a test to ensure that the data would not

be affected. A sample I-V curve was performed on the same thick oxide Pre-Poly device in both the probe station and cryostat. As Fig 6.1 illustrates, the measurement in each case produced virtually the same result.

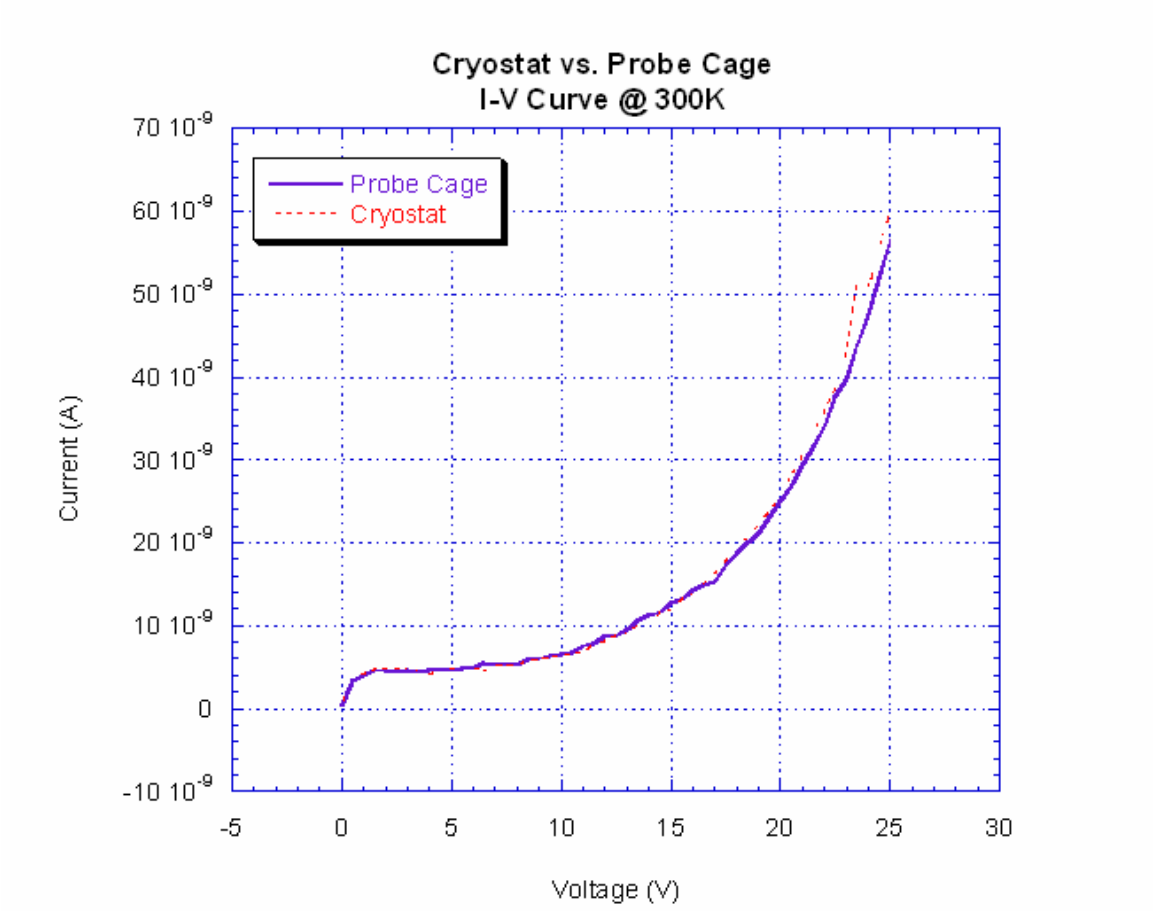

Fig 6.1 I-V test in probe station and cryostat.

6.2.2 Procedures

The C-V characteristics of these capacitors were studied at both forward and reverse biases as well as at temperatures ranging from 300K down to 100K. The forward bias ranges for measurements were typically limited to the working voltage range of the capacitor being studied. Reverse bias ranges were dependent on the temperature of the

measurement as they tended to be very limited. These devices have large values of capacitance; therefore the LCR meter was set to a series resistance capacitance model [47]. The frequency was set to either of the capacitor industry standard frequencies for testing, which are 120Hz and 1kHz. Nominal capacitance measurements were the initial as well as final measurements made on all devices. They were made, at both frequencies, to help monitor any damage being done to the capacitors. C-V curves were made using the automatic sweep function of the LCR meter. Based on manual observation of capacitance values under applied bias, and the maximum delay time of the LCR meter, the delay between measurements was set at approximately 10 minutes.

When making any measurements as a function of temperature, the LakeShore 311 temperature controller was used in conjunction with the cryostat. The Dewar tank of the cryostat was used to hold a supply of liquid nitrogen. A rotary pump was used to keep the cryostat test chamber at a rough vacuum while an electromagnetic pump was used to siphon liquid nitrogen through the tubing in the chamber. A Variac power supply was used to control the strength of the electromagnetic pump and was the only way to control the rate of cooling of the system. The temperature controller used a thermocouple temperature sensor and a resistive heater inside the cryostat chamber to stabilize the system to a preset temperature. The theoretical limit of the system was 77K (liquid nitrogen temperature); however, due to time and liquid nitrogen supply constraints, the system was only able to stabilize temperatures down to 100K with any regularity.

I-V characteristics were also studied at forward and reverse biases over temperatures ranging from 300K down to 100K. As with the C-V measurements, the

forward bias range was limited by the capacitor's working voltage while the reverse bias range varied depending on the temperature of the measurement. In setting up the HP4156B, the current compliance was set to 100uA to prevent too much leakage current during reverse bias measurements. The sampling interval was set to the maximum integration time of 1.6s to filter out as much noise as possible from the measurements. The delay time between measurements was set to the maximum value of 65s to allow as much of a current decay as possible at each voltage level. This was done in order to measure conduction current with as little displacement current as possible. I-t measurements were also performed using the HP4156B. The sampling interval was set, based on the maximum integration time, to be 3.5s between data points. The bias applied and the total length of the measurement varied depending on what was being investigated.

6.3 Types of Devices

The two main classifications of devices that were studied were In-Situ and Pre-Polymerized capacitors. Both types are modern tantalum capacitors that use an identical Ta anode structure and a p-type PEDOT cathode. The distinguishing difference between the two is how the PEDOT is polymerized and applied during the manufacturing process. The In-Situ capacitors go through a dip and dry process, very similar to the application of MnO_2, in which the PEDOT is polymerized in place on the capacitor. The Pre-Poly capacitors have the PEDOT polymerized before it is applied, and then go through a similar dip and dry method to achieve the appropriate cathode thickness.

Within each of these main classifications, there are also several variants of these capacitors that were examined as well. In both In-Situ and Pre-Poly types there were several working voltage ranges, mainly 2.5V, 20V, and 25V. The working voltages are the ranges within which each capacitor can be safely operated. From a device construction point of view, these voltage ranges can be related to dielectric thickness. A certain dielectric thickness is required to be able to support these working voltage ranges. Recall from Chapter 3, that the dielectric thickness is determined by the formation voltage during the manufacturing process at approximately 18 angstroms/volt of formation voltage. This in turn gives the 2.5V and 20V capacitors a dielectric thickness of 180 and 1,480 angstroms respectively, while the 25V capacitors have a dielectric thickness of 1,860 angstroms. The terms working and formation voltage come from the capacitor industry. Since we will be examining these capacitors as MIS devices we will instead discuss them in terms of oxide thicknesses, meaning that 2.5V capacitors are thin oxide devices while 20V and 25V capacitors are thick oxide devices.

KEMET Electronics Corporation provided us with two additional categories of devices that fall within the ranges discussed above, but are in different stages of the manufacturing process. Initially we were given finished capacitors of both In-Situ and Pre-Poly types that had thick oxides with a working voltage of 25V. These devices were used in setting up measurement parameters for the various characteristic tests. Later we were also given a large variety of solid test capacitors. Capacitors in solid test form are those that have been completed but not yet packaged. We received In-Situ and Pre-Poly

solid test capacitors with working voltages of 2.5V and 20V. It was the solid test capacitors on which we performed the bulk of our characteristic tests.

6.4 C-V Characteristics

As previously stated, one of the main goals of this thesis is to investigate whether modern tantalum capacitors behave like MIS systems. Since these capacitors are complex discrete devices when compared to the planar MIS model, we need to be sure that we measure them properly in order to obtain useful data. As discussed above, KEMET Electronics Corporation provided us with several types of these capacitors; due to the relatively manual nature of how these measurements are performed it would be impossible to investigate every single type completely. Therefore, we needed to determine which capacitors would yield the most significant results that could in turn help to broadly describe the behavior these capacitors. It was clear that we must investigate both In-Situ and Pre-Poly devices. It was also reasonable that we only look at solid test devices because they represent the purest form of the capacitor available to us, containing only the anode, dielectric, and cathode structures. The completed packaged parts go through several additional manufacturing steps and contain additional materials that serve the purpose of protecting and structurally supporting the capacitors during usage. The thickest oxide capacitors have a dielectric thickness on the order of 2000 angstroms, while the thinnest are on the order of 200 angstroms. When examining silicon-based MIS systems with similar dielectric thicknesses, it is clear that the effect of applied bias on capacitance is much more pronounced in the thin oxide devices.

The results of simulated C-V Curves using Silvaco software in Fig 6.2 illustrate the difference between a thick oxide and thin oxide device in silicon-based technology. Silvaco is semiconductor process simulation package that can be used to simulate and test semiconductor devices. The result in Fig 6.2 was simulated on two basic silicon-based MIS capacitors of varying oxide thicknesses with p-type substrates. The oxide thicknesses of these devices were chosen to represent the thinnest and thickest oxide capacitors we received from KEMET. The first curve (200 angstroms) shows a large decrease in capacitance as the voltage is swept from negative to positive. This decrease represents the shift from an accumulation of majority carriers to the formation of a depletion region near the semiconductor-oxide interface. According to MIS Theory, the total capacitance of the device is a series combination of the oxide capacitance and depletion capacitance. Therefore, as the bias increases so does the depletion width, causing the depletion capacitance, and the overall capacitance, to decrease. The second curve (2000 angstroms), in comparison, shows a very small decrease in capacitance as the voltage is swept. While the thick oxide device experiences the formation of a depletion region, the overall depletion width is very small when compared to the oxide thickness. Therefore, the effect on capacitance in the thick oxide device is essentially negligible. Since the result in Fig 6.2 is a simplified representation of how we believe the solid test Ta capacitors will behave, it is reasonable from a theoretical point of view to only consider thin oxide devices when investigating C-V characteristics. Therefore, the devices we focused on when examining C-V characteristics were the thin oxide (180 angstrom) solid test devices in both In-Situ and Pre-Poly.

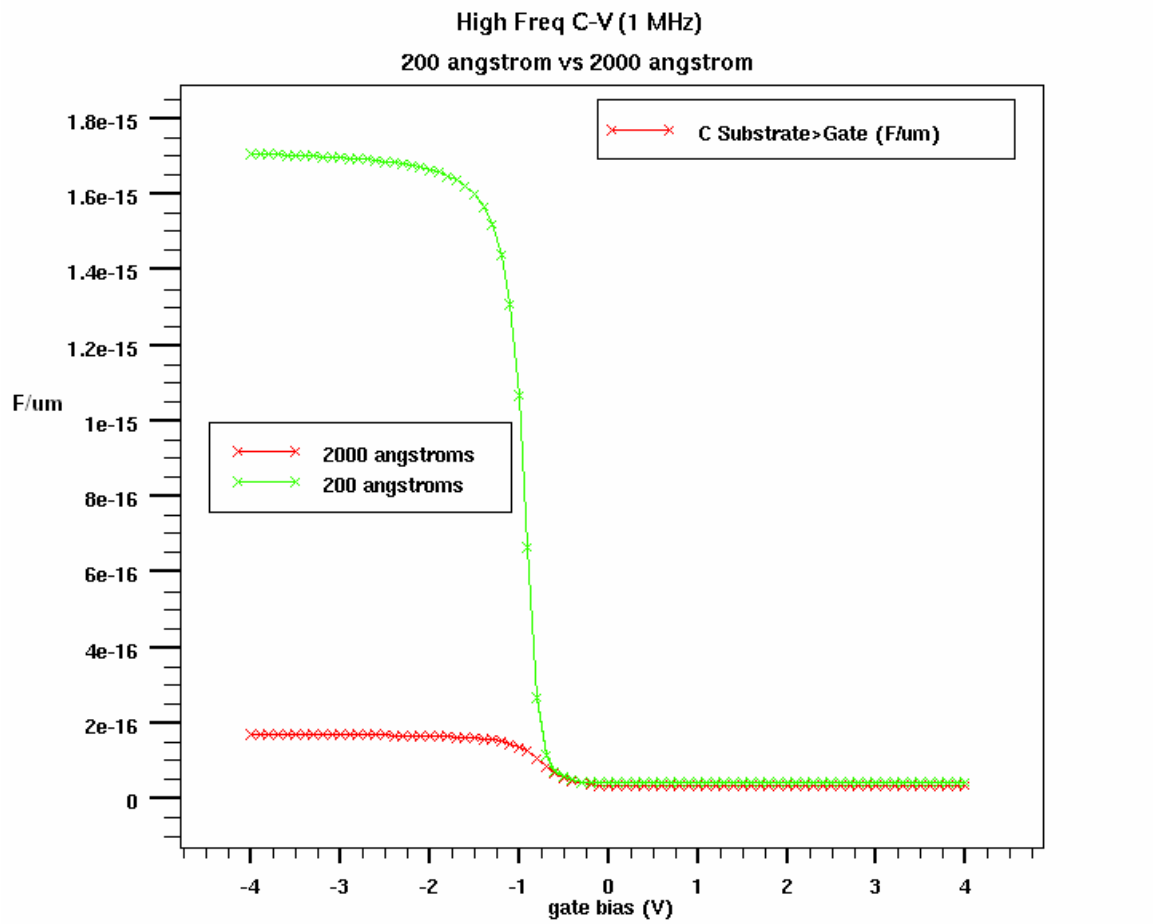

Fig 6.2 Simulated C-V curve of thick oxide and thin oxide MIS devices.

When a bias is applied there is a significant amount of transient response associated with it. In order to take these transient effects into account, we must incorporate enough of a delay time between bias points when making a C-V Curve to allow most of the displacement current to discharge. Based on observations of the measured capacitance under applied bias, 10 minutes appeared to be sufficient for the transient effects to decay. In order to confirm this, a measurement of capacitance versus time was made with the application of an external bias of 2.5V occurring at t=0. Fig 6.3 shows that the capacitance became essentially constant after 10 minutes, thus confirming

that a delay of 10 minutes between measurements is reasonable for C-V measurements. This delay time represents the amount of time that a bias will be applied before a data point is recorded and the bias increases again.

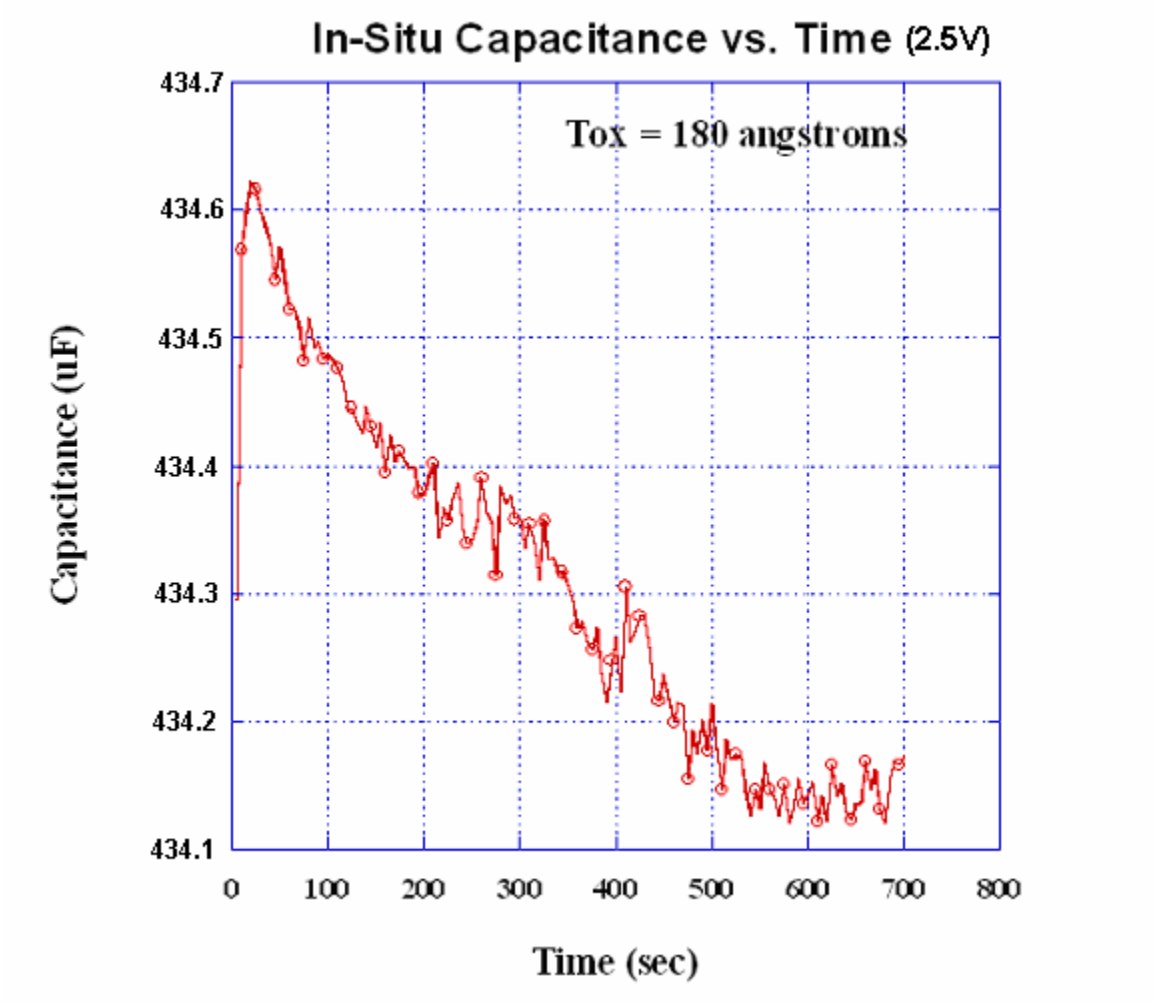

Fig 6.3 Capacitance versus time under applied bias.

6.4.1 Low Temperature Measurements

As discussed above, C-V measurements were performed primarily on thin oxide solid test devices. The thin oxide devices have a working voltage of 2.5V, meaning that they are rated for normal operation up to 2.5V, in forward bias, with a maximum of 3.3V.

These capacitors are not really intended to be operated in reverse bias, but they can be biased up to a maximum of -1.5V. However, the recommendations from KEMET Electronics Corporation are that reverse bias voltages remain much lower than this value due to the high amounts of leakage current observed at those levels. In order to better understand the C-V characteristics of these devices, we first made C-V measurements at low temperatures. The purpose of these measurements was to suppress the leakage current enough to increase the operational range of the devices. This should allow us to observe all modes of operation in the C-V curve.

When examining the devices at 100K, we made a relatively safe assumption that the operational range could be extended beyond the normal forward bias maximum at room temperature (3.3V) in both forward and reverse biases. The bias was swept from positive to negative to avoid driving the device into deep depletion. For each type of device we repeated the measurement on three separate capacitors. From Fig 6.4 for In-Situ and Fig 6.5 for Pre-Poly, we see that the capacitance of the devices appears to have some dependency on voltage as originally suggested.

When looking at these two sets of curves, distinct similarities can be noticed between them and the theoretical C-V curve illustrated in Fig 4.14. They all appear to have a minimum capacitance value near the zero bias point, as well as an increase in capacitance in either bias direction corresponding to Depletion and Inversion modes. From the zero bias point, as the bias decreases, the capacitance increases showing evidence of a depletion region that is decreasing in width. As the bias increases from the zero bias point, the capacitance increases again displaying characteristics of an MIS

device transitioning from Depletion mode to Inversion mode, at a moderately low frequency. In the reverse bias region, the curves appear to show Depletion mode behavior but never quite saturates to C_{OX} in Accumulation mode. In the forward bias region, what appears to be the Inversion mode is consistent with a measurement between high frequency and quasi-static. In a quasi-static measurement the variations in the applied bias cause variations in the inversion charge that eventually bring the capacitance back to C_{OX}. In a high frequency measurement the thermally generated minority carriers respond much too slowly to support the variation in applied bias. The variation of charge must then be supported by the depletion charge causing the capacitance to settle to C_{MIN} at the maximum depletion width. We do not observe a forward bias saturation to either C_{OX} or C_{MIN} in Fig 6.4 or Fig 6.5 at 120Hz within this bias range.

While the measurements shown in Fig 6.4 and Fig 6.5 display definite similarities to a theoretical C-V curve of an MIS device, they appear to show only a portion of the entire picture. Perhaps the largest difference from theory is that both In-Situ and Pre-Poly devices fail to reach a constant capacitance value in either the Accumulation or Inversion mode. Conducting these measurements at low temperatures does appear to extend the operational range of these devices significantly. However, as most clearly displayed in the Pre-Poly devices at biases less than -4V, higher fields seem to cause adverse effects, most likely attributed to leakage current, preventing us from observing saturation to C_{OX}. It is possible that the field needed to reach the oxide capacitance in these devices is so high that the associated level of leakage current would cause the devices to fail, and, therefore, C_{OX} could never be observed.

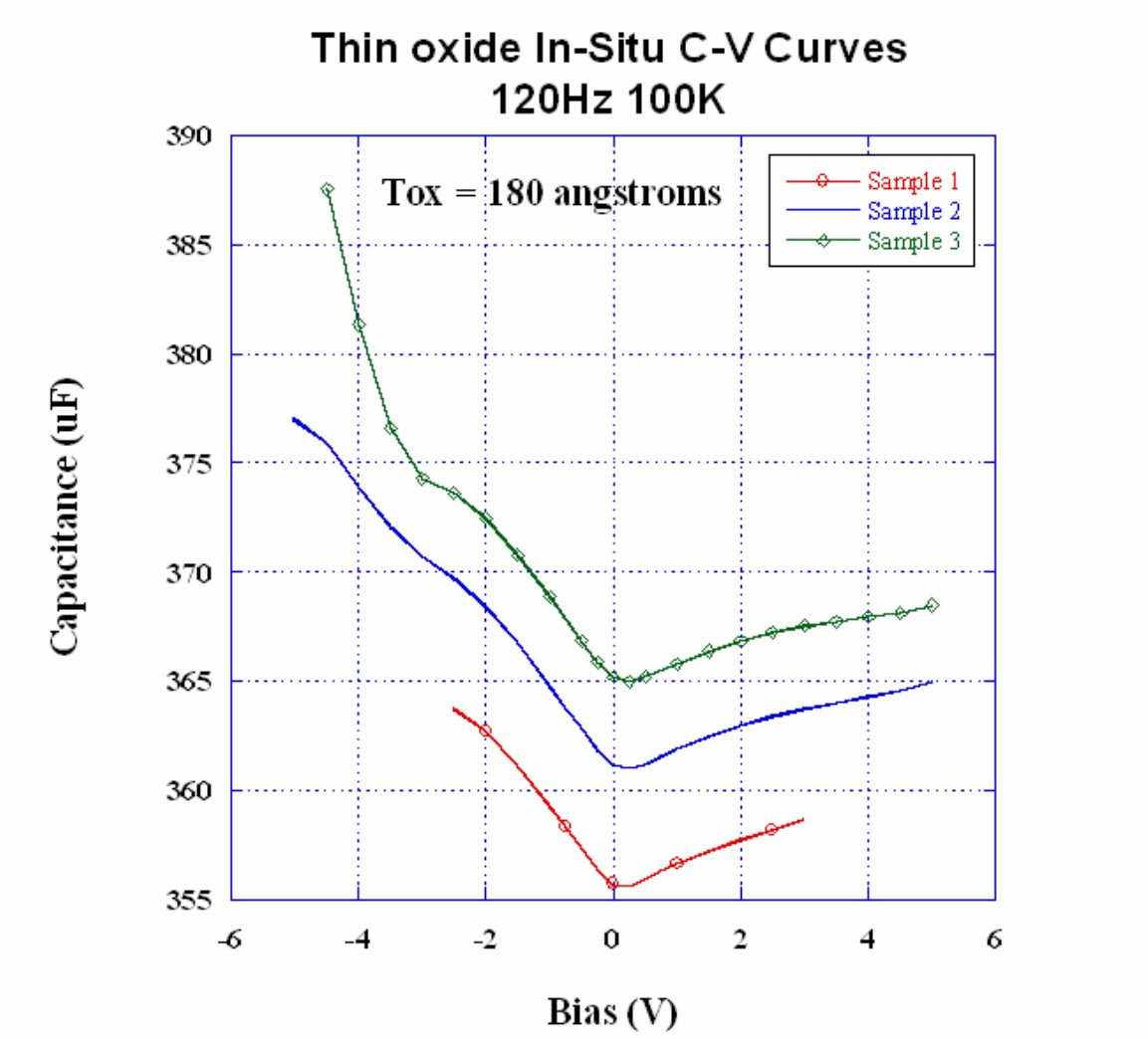

Fig 6.4 In-Situ C-V curves at 100K.

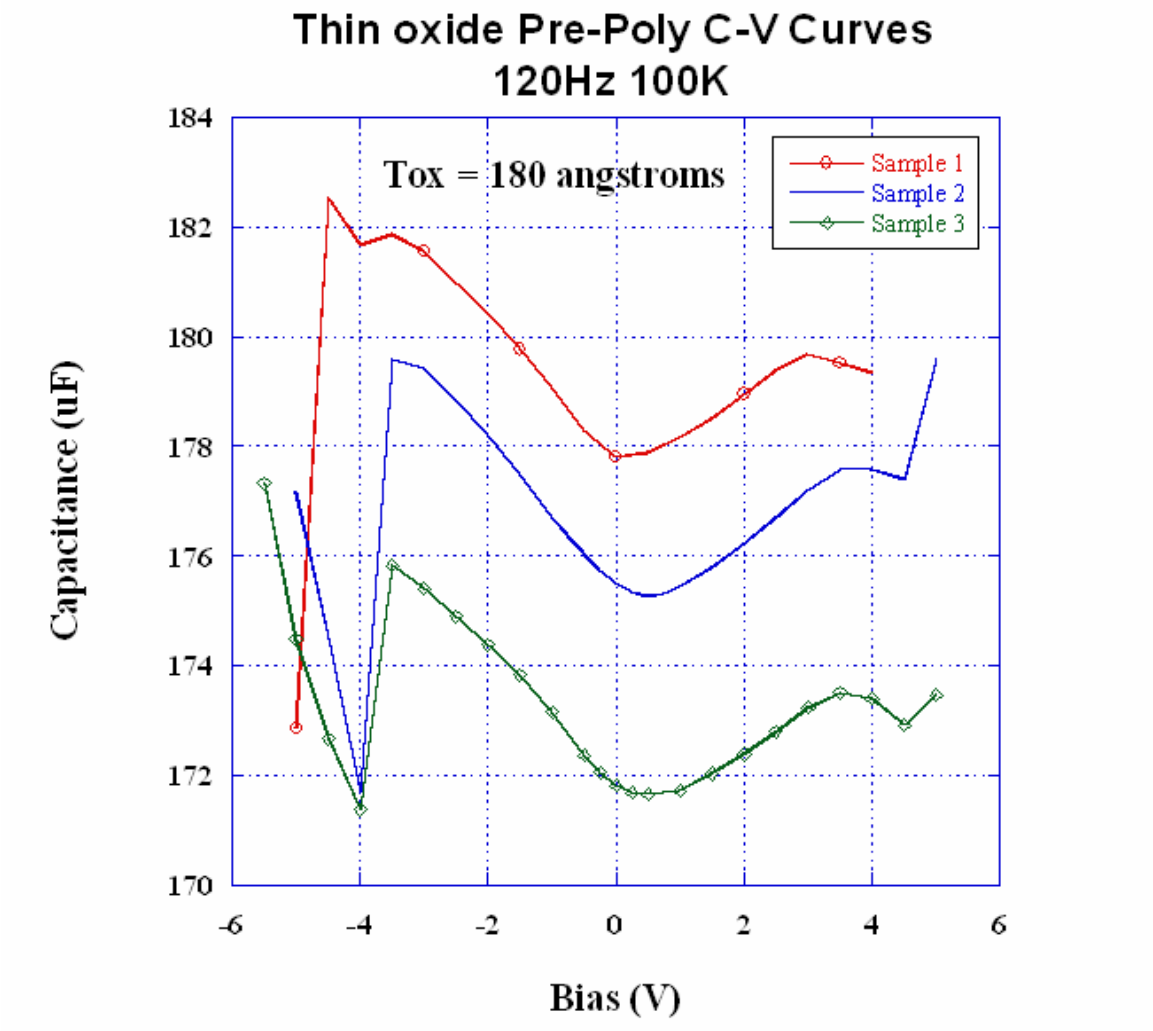

Fig 6.5 Pre-Poly C-V curves at 100K.

6.4.2 Temperature Dependence

When comparing Fig 6.4 to Fig 6.5 one thing to notice is that the values of capacitance between figures are very different. While In-Situ and Pre-Poly devices are manufactured in slightly different ways, they are still intended to have equivalent capacitance at zero bias. In Table 6.1 we compare the zero bias capacitance at 100K to the initial nominal capacitance measurements made at room temperature. The initial

measurements show that the capacitances of all six devices vary but still fall within a relatively small range. The 100K measurements show an even smaller range within each type of capacitor but a large difference between types. Also, while the initial nominal measurements do not vary greatly between types, at 100K the zero bias capacitance of the Pre-Poly devices are approximately half that of the In-Situ devices. It is clear that the capacitance of each type of device has a different dependence on temperature.

Table 6.1 Initial nominal capacitance versus 100K zero bias capacitance.

Pre-Poly Capacitors	Initial Nominal Capacitance (120Hz)	100K Zero Bias Capacitance (120Hz)
Sample 1	458.5uF	177.8uF
Sample 2	455.9uF	175.5uF
Sample 3	424.1uF	171.8uF
In-Situ Capacitors		
Sample 1	482.3uF	355.7uF
Sample 2	500.0uF	361.2uF
Sample 3	495.1uF	365.2uF

In Table 6.1 we show an indication of the temperature dependence of these devices, but it only gives the two extremes of the overall range in which we are investigating. These capacitors are not designed for, or normally operated at, cryogenic temperatures. Therefore, in order to relate any information from 100K measurements to normal operating ranges, we must observe how capacitance is affected by temperature. In Fig 6.6 we show the zero bias capacitance measurements of both types of devices as a function of temperature. This particular measurement was made on virgin devices by

cooling each of them to 100K and slowly warming them to 300K while taking periodic capacitance readings.

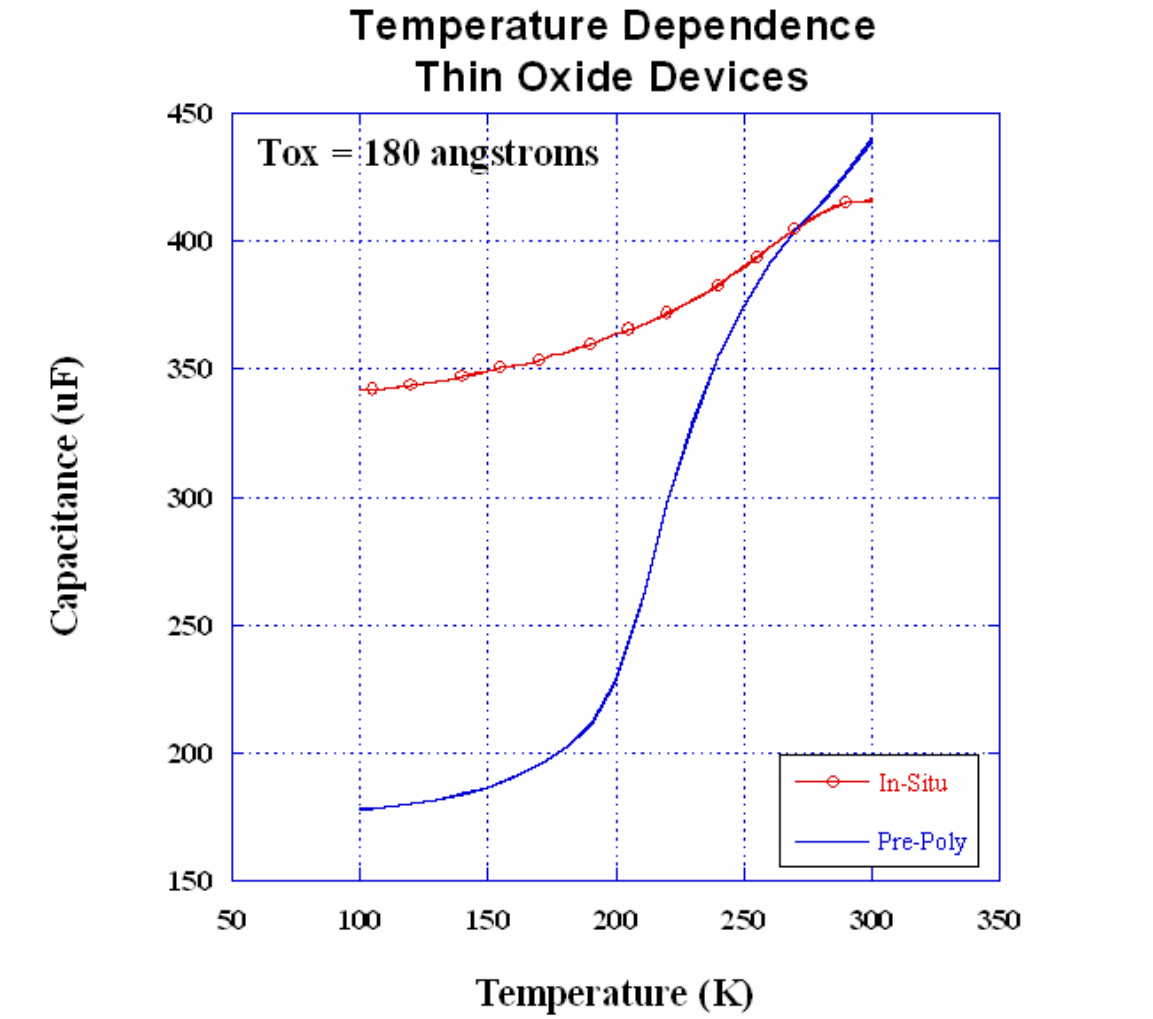

Fig 6.6 Temperature dependence of thin oxide In-Situ and Pre-Poly devices.

It is clear that both capacitor types have significant temperature dependence. However, the temperature dependence of the Pre-Poly device seems to be much more significant than the In-Situ device. The only difference between these types of capacitors exists in the application and polymerization of their PEDOT cathode. The effects of this

difference are exaggerated by macro defects in the Ta_2O_5 anodic film, such as pores and cracks. PEDOT molecules formed by In-Situ polymerization are small enough to penetrate these defects, while those formed by Pre-Polymerization are typically larger than the defects and stay on the dielectric surface [48].

We know, from KEMET, that solid test capacitors contain a slight amount of moisture that is reduced in a subsequent high temperature step in the manufacturing process. This small amount of moisture could provide one possible answer to the capacitance reduction at low temperatures. The dielectric constant of water, κ_{water}, is 81; however, at cryogenic temperatures these measurements are well below the freezing point of water. Once this moisture has been frozen, its dielectric constant, κ_{ice}, is reduced to 1.

The polymerization process requires several applications to achieve complete coverage. Even so, we know from KEMET that the polymerization coverage is very good but not complete. There are gaps in the polymer layer that leave room for this moisture to be trapped, as illustrated in Fig 6.7. Due to its larger PEDOT molecular size, it is possible that Pre-Poly leaves a larger amount of moisture within the capacitor than In-Situ polymerization [48]. Containing larger amounts of water within the polymer layer would cause a more significant effect in the transition from water to ice and offer an explanation for the larger capacitance drop at low temperatures observed in Pre-Poly devices.

If the capacitance loss between 300K and 100K measurements is due to the transition of trapped moisture from water to ice, then the effects observed in our measurements should be similar to those observed when the moisture is removed from

the system by drying. KEMET performs a thermal drying step in the capacitor manufacturing process that takes place between the solid test devices that we have, and finished packaged parts. Once this step is completed, the dried solid test devices should produce very similar results to our solid test devices at 100K.

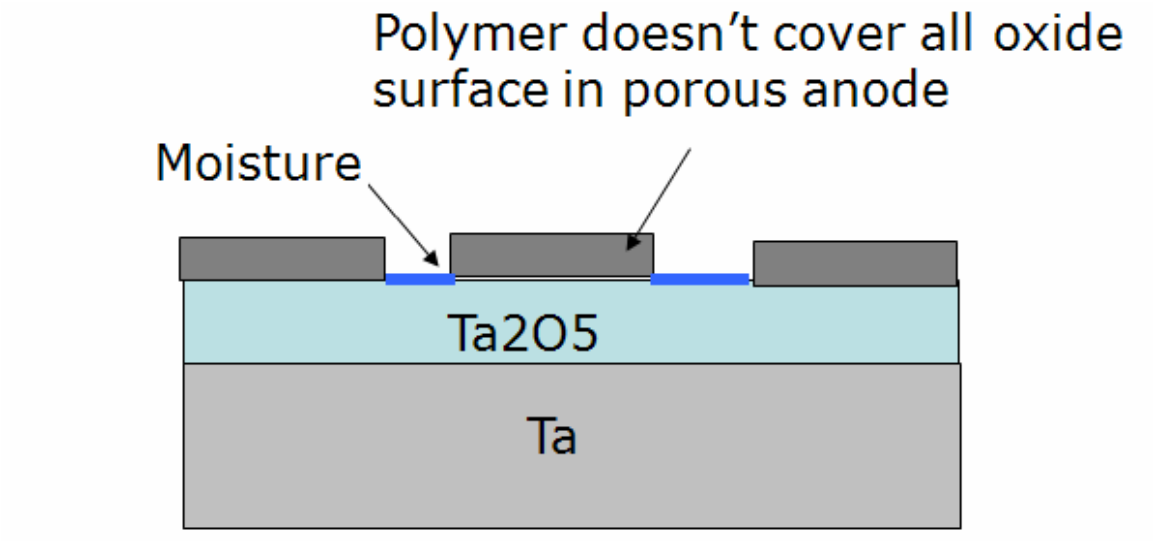

Fig 6.7 Moisture in gaps in Pre-Poly surface.

In Fig 6.8, we show zero bias capacitance versus formation voltage for In-Situ devices at both 300K and 100K. The values of formation voltage were determined by KEMET during the manufacturing process. The data shows that there is a definite capacitance loss with decreasing temperature at all formation voltages. This decrease in capacitance is larger in lower formation voltage, or thin oxide, devices. When recording the data we first made measurements at 300K, and then lowered the temperature to 100K. Afterwards we made a second 300K measurement to show that the process is reversible and the capacitance returned to its starting value. In Fig 6.9, we show the same type of measurement but on Pre-Poly devices. The results again show a decrease in capacitance

at all formation voltages, as well as a greater decrease for the lower voltage devices. However, the overall decrease is much more significant in Pre-Poly devices.

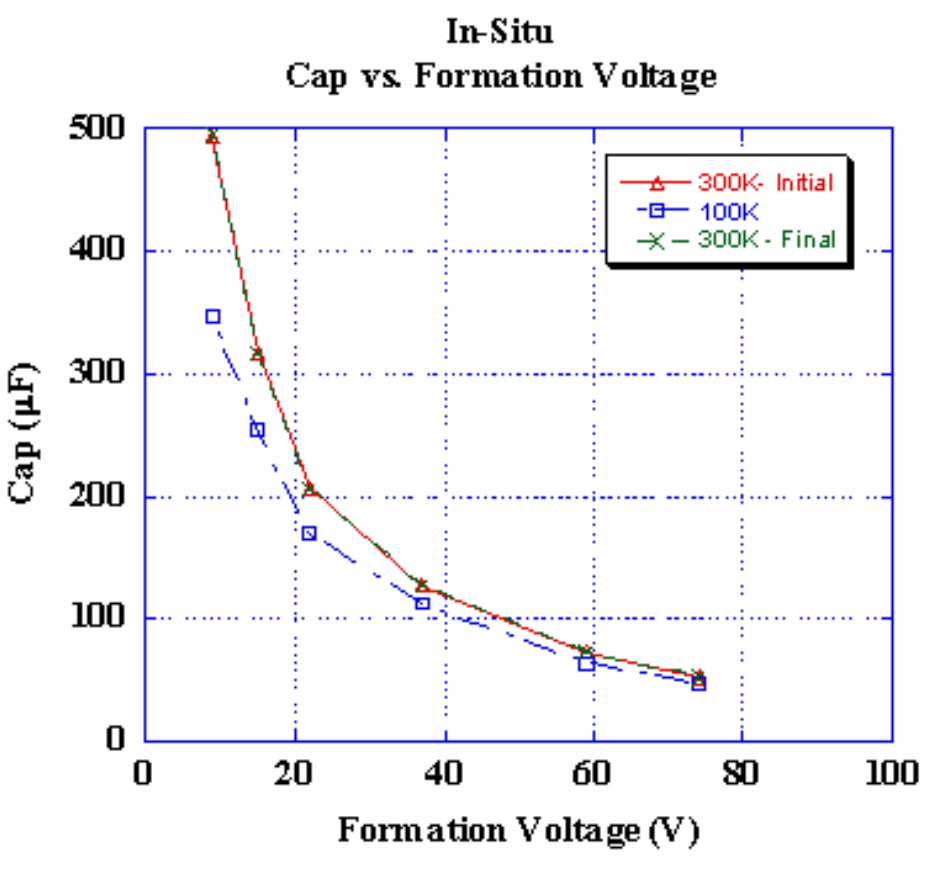

Fig 6.8 Capacitance versus formation voltage for In-Situ devices.

Another way to look at the data presented in Fig 6.8 and Fig 6.9 is to examine the percentage change in the overall capacitance which can be written as,

$$\Delta Cap\% = \frac{|C(300K) - C(100K)|}{C(300K)} \cdot 100\% \qquad (6.1)$$

where *C(*300*K)* is the capacitance at room temperature, *C(*100*K)* is the capacitance at 100K, and Δ*Cap%* is the overall percent change in capacitance.

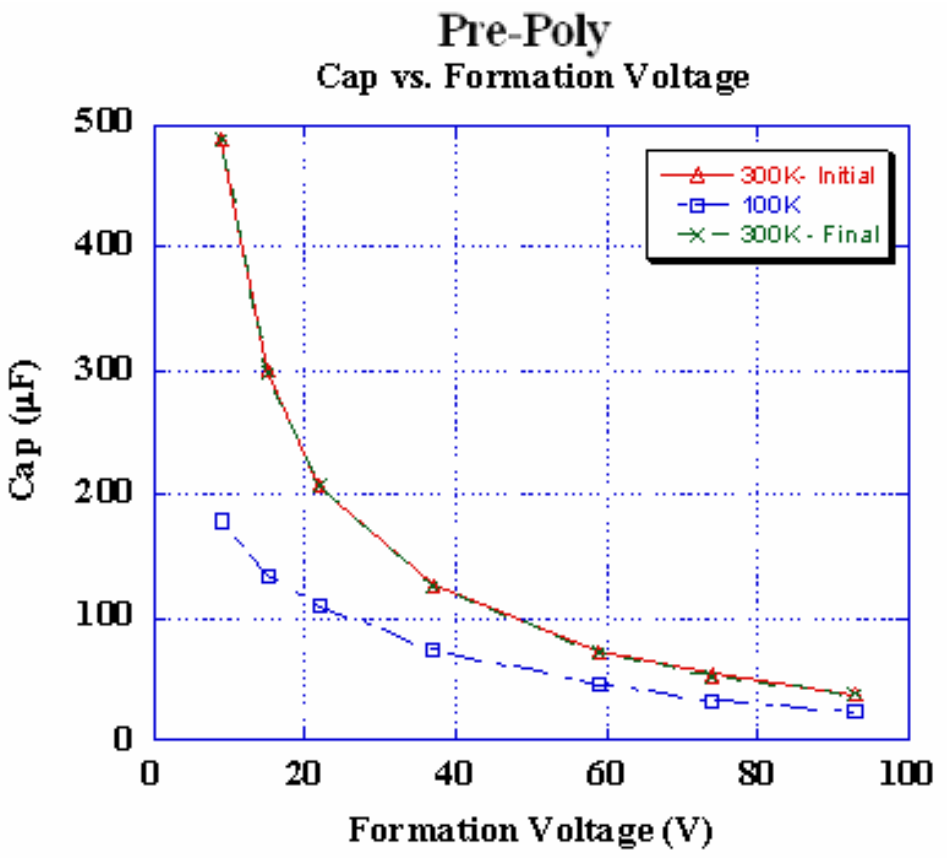

Fig 6.9 Capacitance versus formation voltage for Pre-Poly devices.

In Fig 6.10, we show the percent change in capacitance between 300K and 100K for our In-Situ solid test devices as well as the percent change found by KEMET from a different measurement. The percent change showed by KEMET is the change between a solid test device and a solid test device that has been dried, both of which were made at 300K. The data from KEMET shows that there is approximately a 15% difference in capacitance between solid test and dried solid test at the thinnest oxide thickness, and approximately a 5% difference for the thicker oxide devices. There is almost a 30% difference in capacitance between our solid test devices at 300K and 100K for the

thinnest oxide down to about a 10% difference in the thickest oxide devices. In Fig 6.11, we show similar curves for the Pre-Poly devices. The KEMET results show over a 60% change in capacitance for the thinnest oxide devices, and over a 30% change for the thickest oxide devices. Our results show over a 60% change for the thinnest oxide devices, and almost a 35% change for the thickest oxide devices.

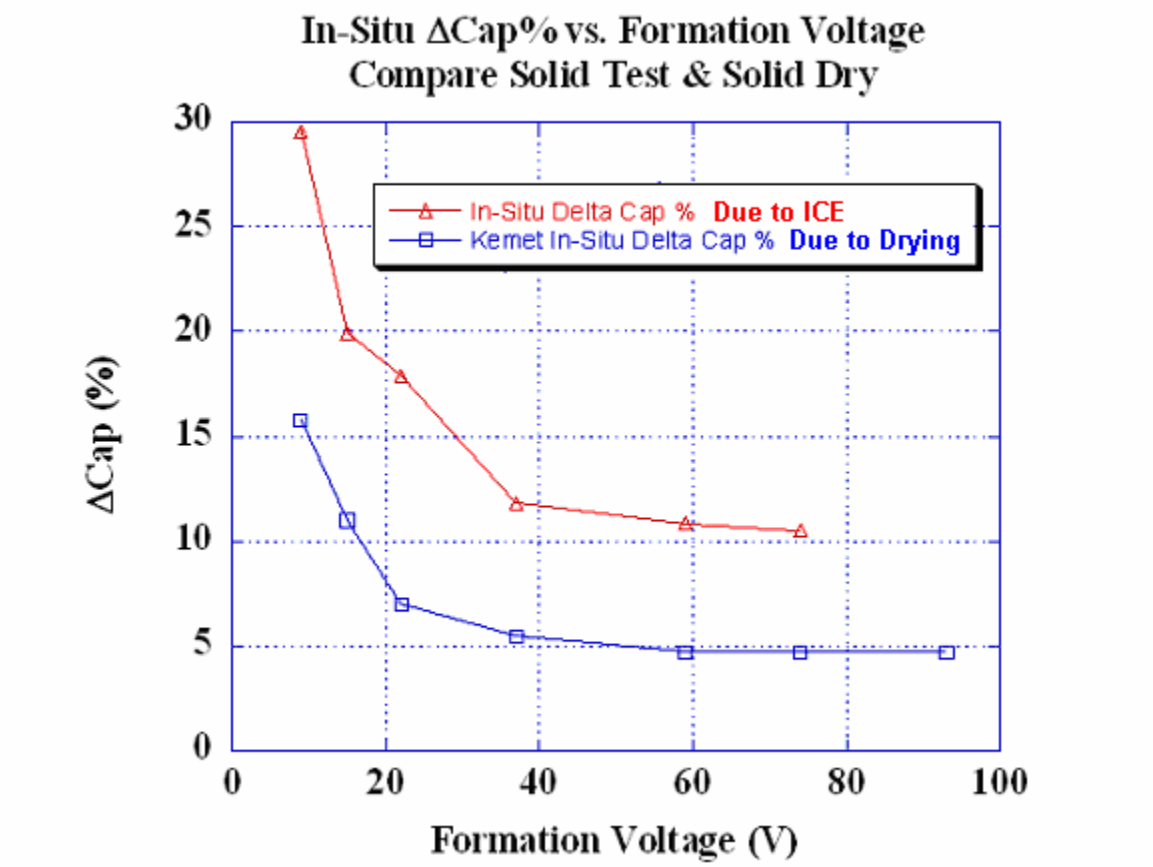

Fig 6.10 Percent change in capacitance for In-Situ devices.

Both Fig 6.10 and Fig 6.11 support the theory that there is moisture trapped in gaps in the polymer layer, illustrated in Fig 6.7. As this moisture is frozen or removed by drying, the associated area is effectively removed from the system, resulting in Pre-Poly

capacitance loss. In both In-Situ and Pre-Poly devices there is a significant change in capacitance observed after the KEMET drying process, as well as after cooling the devices to 100K in our experiments. This capacitance change is much more significant in the Pre-Poly devices than in In-Situ ones, which is consistent with the theory that Pre-Polymerization traps more moisture in the polymer layer. We also know from KEMET that the drying process does not completely remove all the moisture from the device. However, at 100K, all of the moisture in the device will be frozen. This observation is confirmed in Fig 6.10 and Fig 6.11. In both figures the effect of cooling the devices has an effect that is equal to or stronger than the effect of drying the devices.

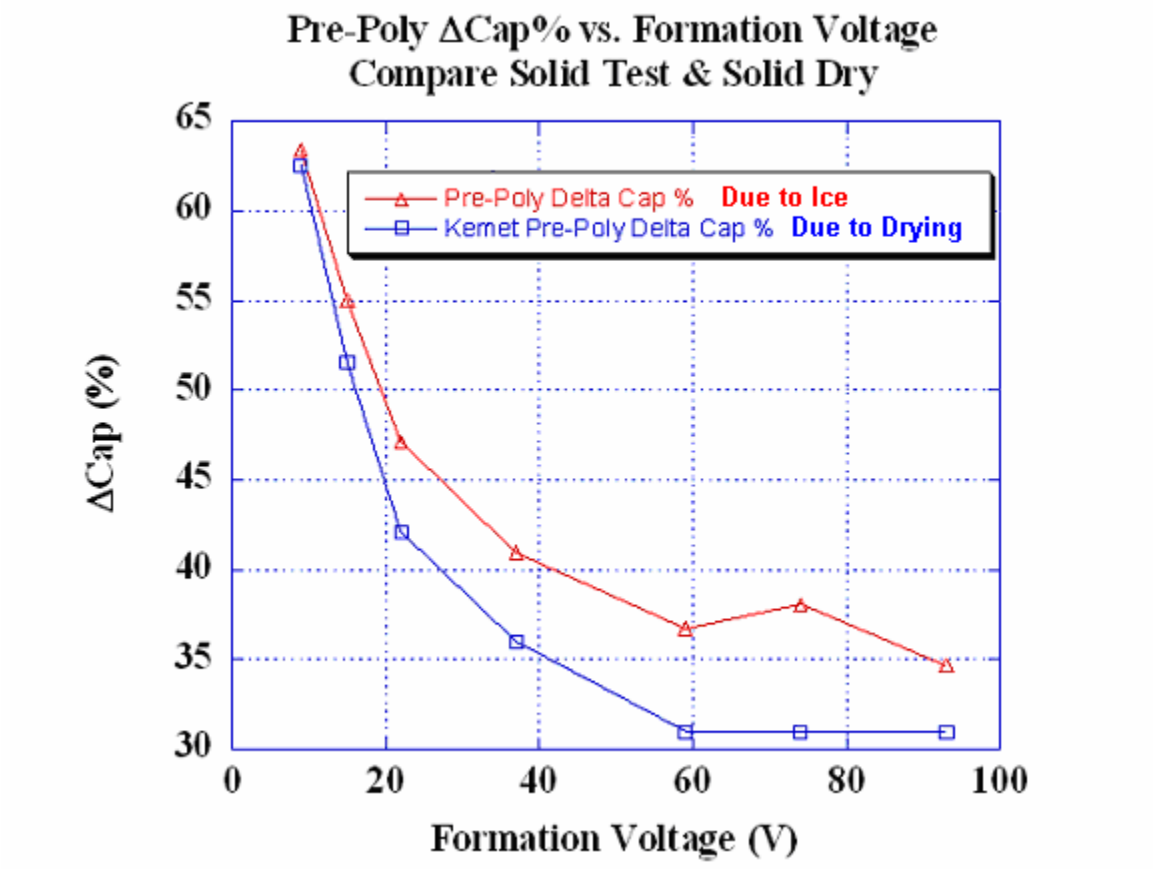

Fig 6.11 Percent change in capacitance for Pre-Poly devices.

Low temperature C-V measurements revealed that the capacitance of these devices is indeed voltage dependent, and they provided evidence that this voltage dependency can be qualitatively explained by MIS theory. However, as previously stated, these devices are not normally operated at such extreme temperatures, and as Fig 6.6 shows, their temperature dependence is quite complex. Therefore, even if we were to observe C_{OX} at these temperatures, we would be unable to relate it to normal device operation without first fully understanding the temperature dependency.

6.4.3 Room Temperature Measurements

C-V measurements were made at room temperature (300K) on both thin oxide In-Situ and Pre-Poly devices. This temperature falls within the normal operating range for these devices. Therefore, measurements were made within the recommended bias range which is between -1.5V and 3.3V. It is expected that outside of this bias range there is a high probability that measurements would be significantly affected by leakage current. The measurements were swept from positive to negative bias and were performed on the same six devices as the low temperature measurements.

The C-V curves in Fig 6.12 and Fig 6.13 appear quite different from their low temperature counterparts. In both types of devices there is a large increase in capacitance with an increase in reverse bias. This increase occurs, almost without bound, until the LCR meter registers an overload reading and is due to the large amount of leakage current present in reverse bias. While the most noticeable effect in these curves is caused by excessive leakage current, the figures also share a few similarities with low temperature and theoretical C-V curves.

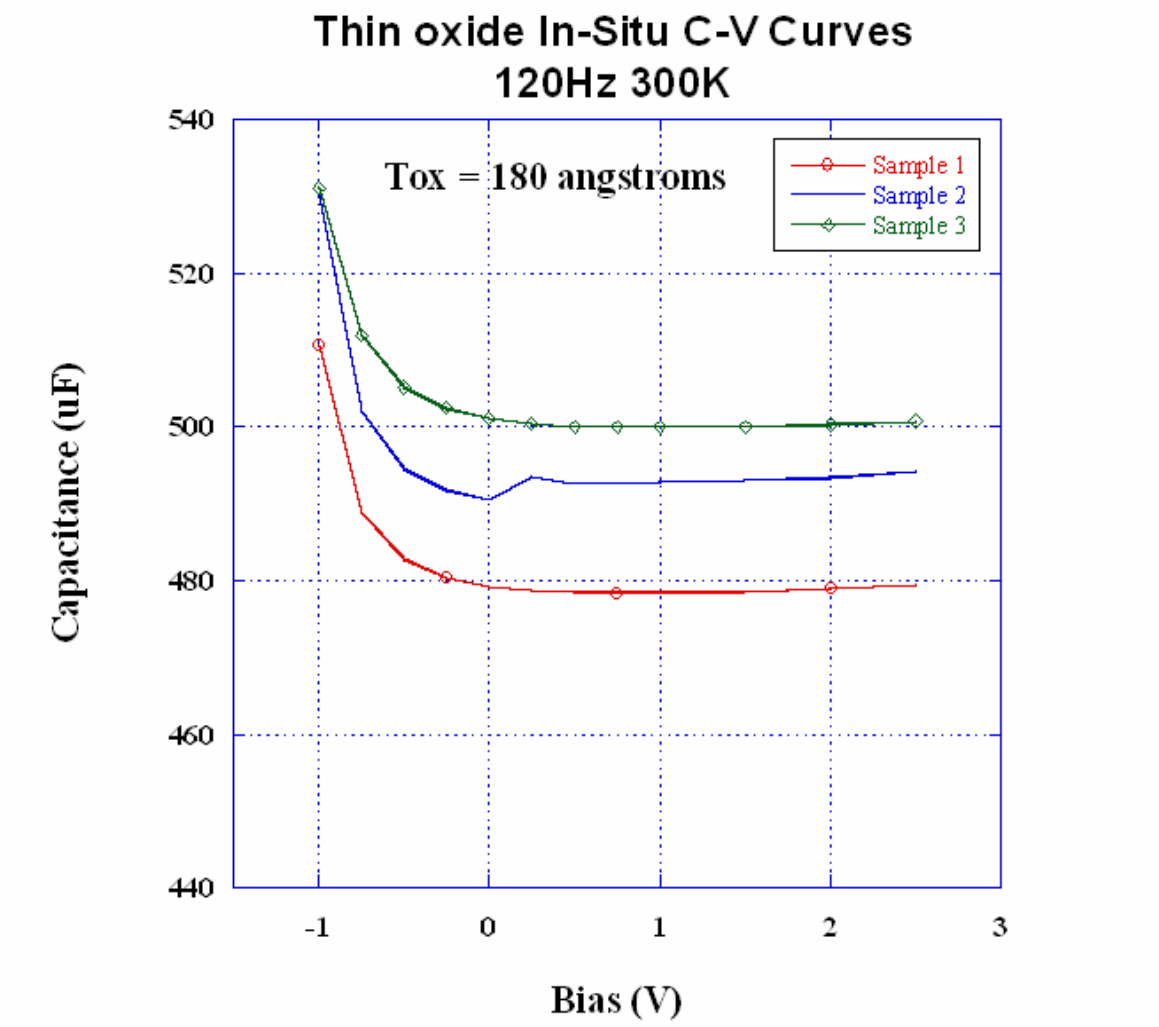

Fig 6.12 In-Situ C-V curves at 300K.

With only a few exceptions, the capacitors reach a minimum capacitance value at a slight forward bias. This is consistent with the C_{MIN} observed in low temperature measurements and the maximum depletion width predicted by MIS theory. From a slightly positive bias to a slightly negative bias a gradual increase in capacitance is noticeable, which is consistent with Depletion mode. However, the leakage current eventually takes over and causes the capacitance to spike, making it impossible to

observe the Accumulation mode or C_{OX}. As we look further into the forward bias direction we see a small increase in capacitance in most of the curves. This observation is consistent with the Inversion mode in a C-V curve made at a frequency that is low but not quasi-static. An interesting comparison between 300K and 100K measurements is that at low temperature the capacitance appeared to increase much more in inversion than it did at room temperature.

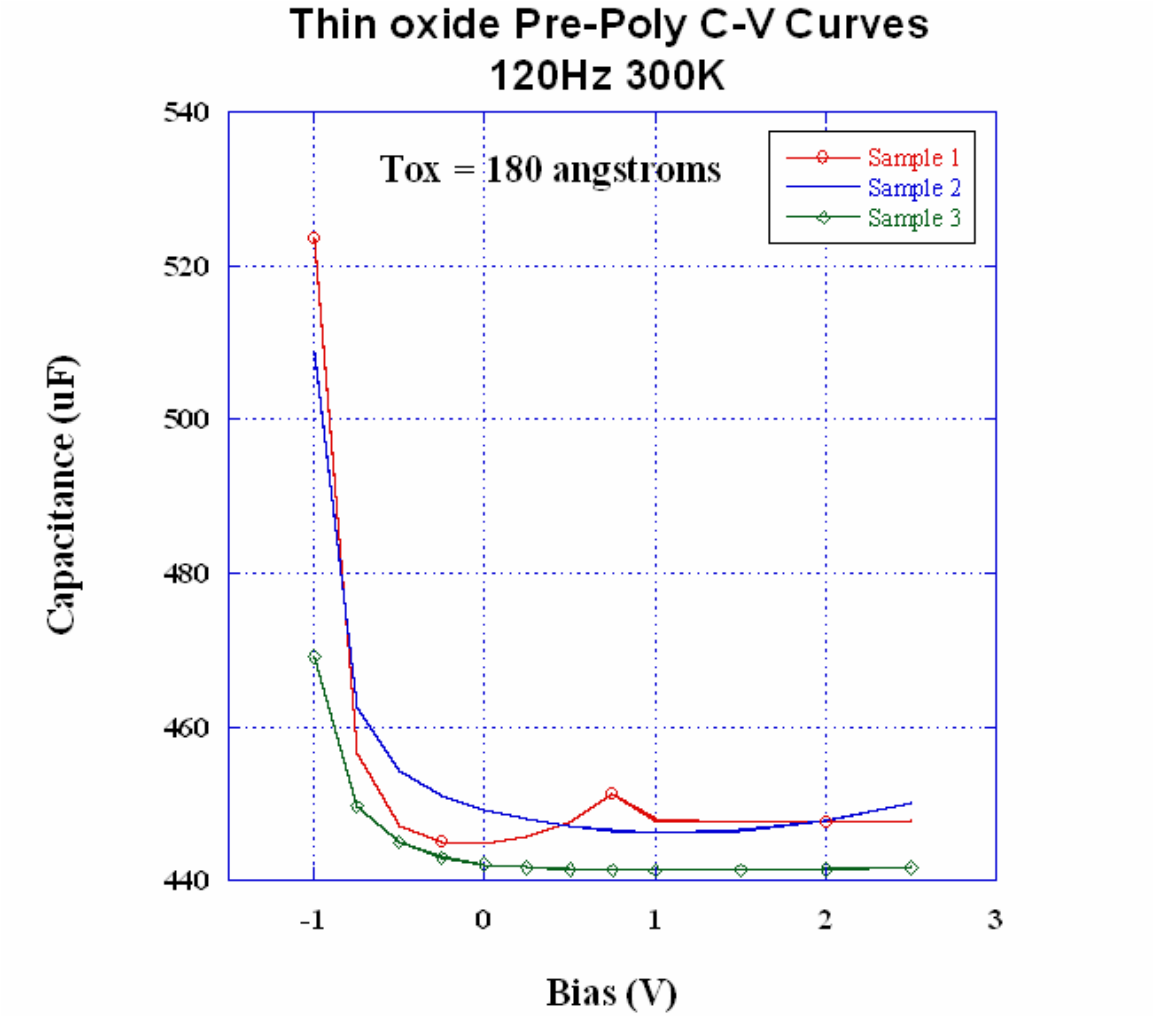

Fig 6.13 Pre-Poly C-V curves at 300K.

The In-Situ curves in Fig 6.12 show a fairly reasonable range of capacitance values between samples and each curve appears to have a similar shape. The Pre-Poly curves in Fig 6.13 also show a reasonable distribution of capacitance at every bias point. The capacitance of the Pre-Poly devices is also significantly lower than all of the In-Situ curves. In forward bias the Pre-Poly devices range from approximately 440uF to 450uF while the In-Situ devices range from approximately 480uF to 500uF.

At room temperature we were able to perform measurements over a much smaller voltage range on these devices when compared to low temperature. The capacitance appeared to be less dependent on bias at positive voltages. However, there is still evidence that these devices have tendencies similar to MIS devices. While we can compare them to MIS devices in several ways, it is still evident that these capacitors are much more complicated structures. Instead of planar systems, these devices are distributed networks of spherical capacitors. In turn, they can only be related to MIS theory in a very qualitative way.

6.5 I-V Characteristics

The other goal of this thesis is to identify possible leakage mechanisms in KEMET's modern tantalum capacitors, and compare these results between In-Situ and Pre-Poly types. Since we have shown that these devices can qualitatively be thought of as MIS systems, we will also approach them as such when investigating their I-V characteristics. When examining traditional MIS devices, I-V measurements are made by sweeping an applied bias across the device through a certain voltage range while measuring the associated current. As we have made clear in previous sections, these are

not traditional MIS devices, and as such we must modify most of the measurement parameters. Since the capacitance of these devices is so large, the main parameter we must adjust is the delay time between measured bias points in the sweep. Before we begin setting parameters and making measurements, we must determine which types of devices to characterize. We must investigate both In-Situ and Pre-Poly types to see what leakage current mechanisms are present. Within each of these types of devices we will again make measurements only on solid test capacitors since they are the simplest form of a completed capacitor that we have. There is no reason to exclude particular oxide thicknesses for these experiments as there was when making C-V measurements, so we will investigate both thick oxide and thin oxide devices for both In-Situ and Pre-Poly.

6.5.1 Current-Time Measurements

The ideal situation when making I-V measurements is that the current at each bias point represents only the dc conduction current. We know however, due to the large capacitances of these devices, that it will take a significant amount of time for the transient currents to settle. The settings on the HP4156B limit us to a 65s delay between measurements at applied bias points when making an automatic I-V sweep. In order to observe the true dc conduction current, we must make I-t measurements at each bias point that are long enough for us to observe steady-state current. By making I-t measurements in this manner, we can take the steady-state current from each bias point and manually construct an I-V curve from the sequential set of I-t curves. An I-t curve on a thick oxide Pre-Poly device is shown in Fig 6.14. The measurement was made with a bias of 19V, which is just under its normal operational limit, and the current was

monitored for slightly longer than four hours. The current appears to settle almost to a constant value but is still decaying ever so slightly and needs more time to reach steady-state. Therefore, in order to observe the steady-state current we need to make the I-t measurements in excess of four hours.

While waiting several hours for a stable dc conduction current at each bias would be extremely time-consuming, it is possible. An observation worthy of note, however, is that every I-t measurement places the device under extended stress. Conducting I-t measurements at enough bias points to create an I-V curve would result in a large amount of stress being placed on the device under test. While the device may not necessarily be damaged, it is very likely that the combined stress will affect its overall performance. Manufacturers of solid tantalum capacitors apply extended stress to their devices in order to age them and "self-heal" defects between the dielectric and PEDOT. This aging process consists of placing a constant bias on the capacitors over a long period of time to allow the "self-healing" mechanisms to take place. Conducting a series of long I-t measurements would provide conditions similar to the aging process. Since we are using solid test devices that have not yet undergone the aging process, any extended stress will slightly change the characteristics of the devices. Therefore, even though we are capable of observing the dc conduction current, doing so would ultimately alter the result we are trying to measure.

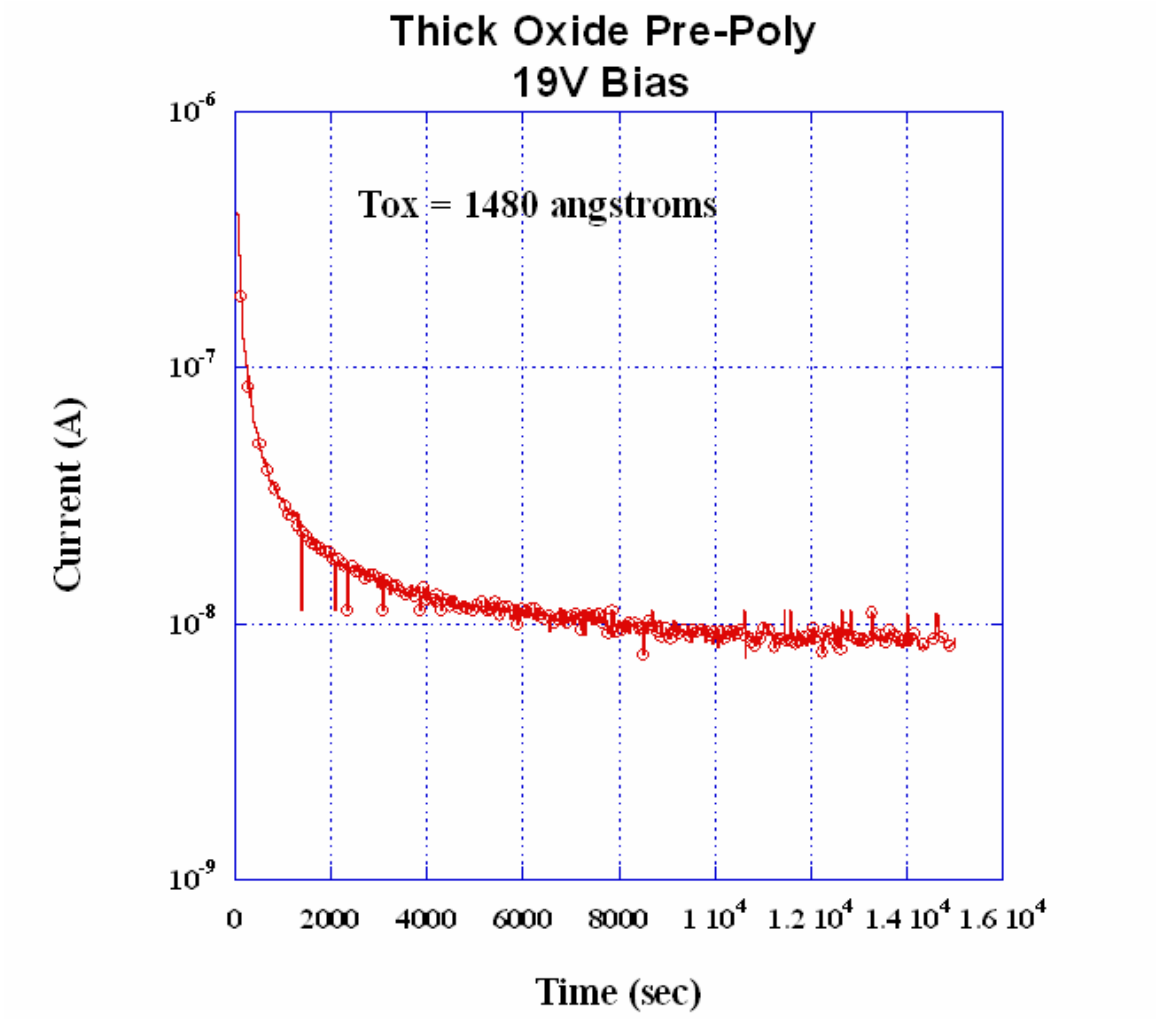

Fig 6.14 I-t measurement on thick oxide Pre-Poly device.

While manually making an I-V curve from a series of I-t measurements should produce the most accurate representation of the dc conduction current, the performance of the device will have changed when comparing the first and final I-t measurements. Fig 6.15 shows an I-t measurement made on a thin oxide In-Situ device. The measurement never decays completely to steady-state, but it is clear that a large amount of the transient current decays away very quickly. The initial current was approximately 28μA and

dropped to 21nA by 65s, the maximum delay time for the HP4156B. This decrease in current is significant enough to occur well beyond the RC time constant of the capacitor and therefore should be long enough to result in a good approximation of the true dc conduction current.

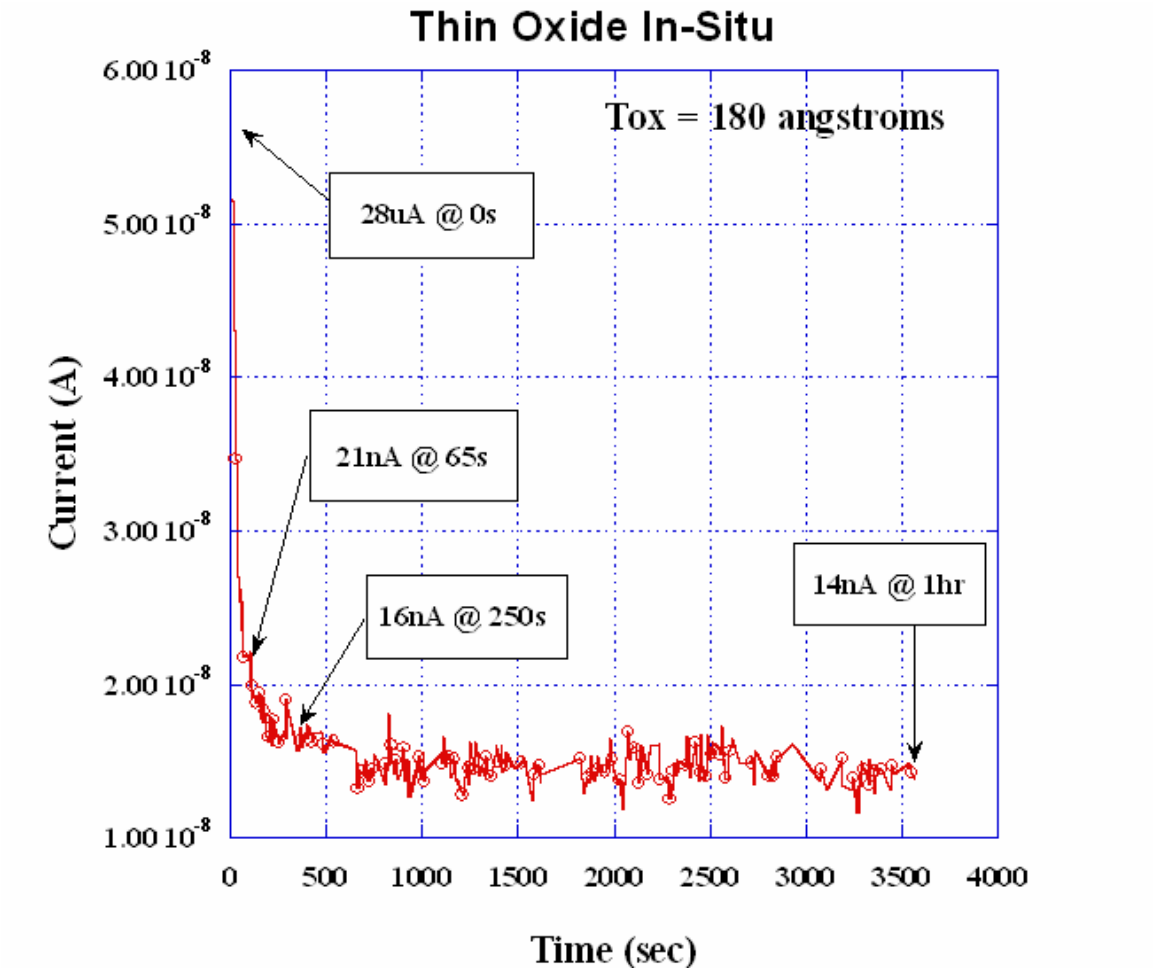

Fig 6.15 I-t measurement on thin oxide In-Situ device.

Delaying the measurement by 65s at each bias point would not allow the device to reach pure dc conduction current. However, according to Fig 6.15, the current only decays from 21nA to 14nA between 65s and 1 hour making it essentially negligible when

compared to the amount that occurs in the first 65s. Performing I-V measurements in this manner should produce a result that has a consistent excess of current at each bias point. The I-V curve should be approximately the same shape as if it were performed manually with I-t measurements. The main difference would be that the magnitude of current recorded would be shifted up slightly by some constant. An example of this type of shift is illustrated in Fig 6.16. In this figure data from two I-V measurements performed on a thick oxide In-Situ device are shown. The bottom I-V curve is based on several separate I-t measurements with a 1 hour settling time. The top curve is an automatic I-V sweep made with a 65s delay between measured points. The manual I-V curve only uses a one-hour delay between measurements, instead of the full delay needed to reach steady-state. This was done in order to minimize the stress on the device.

By using a 65s delay to perform I-V measurements, we were not observing pure dc conduction current of these devices. Therefore, any data we collected was not truly representative of devices to the point where we could extract a complete set of materials and device parameters. However, because these measurements were made with a delay longer than the RC time constant and every point on the I-V curve appeared to be shifted by a constant, we could still make qualitative observations about the types of conduction mechanisms present in these devices.

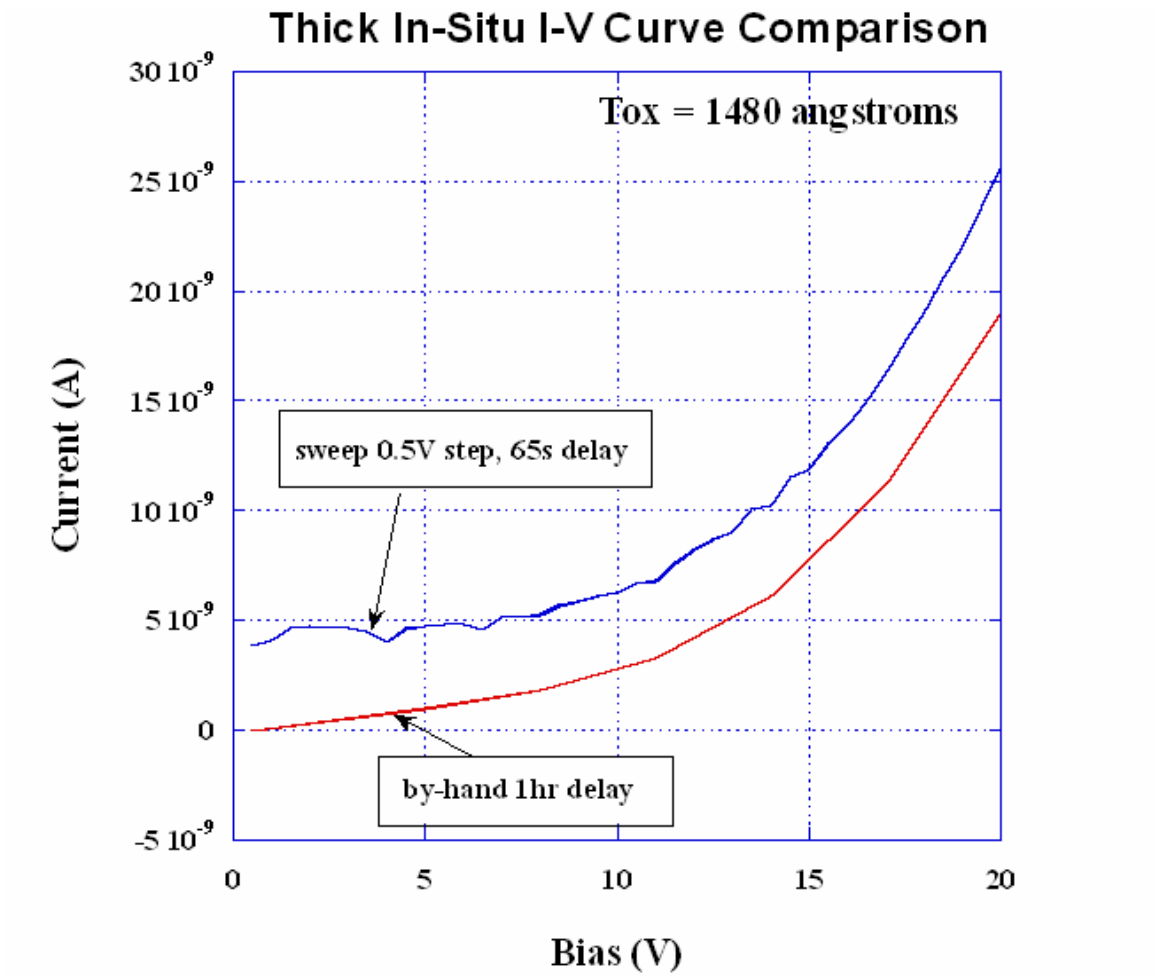

Fig 6.16 Automatic and manual I-V curves.

6.5.2 Temperature Dependence

We know from KEMET and the C-V characteristics previously discussed that these devices are very temperature-dependent. In order to investigate how this temperature dependence relates to their I-V characteristics, we made both forward and reverse bias I-V measurements at various temperatures. These measurements were only made on thick oxide (1480 angstroms) In-Situ and Pre-Poly devices because they have a larger operational range and should provide a greater opportunity to observe variations

with temperature. The temperatures used for the measurements were 300K, 200K, and 100K. The bias ranges were the normal working range of 0-20V for the forward biased regions, and the reverse bias ranges were dictated by the temperature, with a maximum -1V at 300K to the full -20V at 100K.

The forward and reverse bias measurements at the various temperatures were made on one thick oxide In-Situ and one thick oxide Pre-Poly device. At each temperature one forward bias measurement and one reverse bias measurement were made, making a total of six measurements per device. In Fig 6.17 we show all of the measurements from the In-Situ device combined into one graph. As we originally speculated, the most obvious temperature dependence occurs in reverse bias operation. At 300K the leakage current is in the micro amp range at -1V. While at 200K the leakage current is reduced to ~100nA at -10V, and at 100K it is below 10nA at -20V.

The forward bias operation of the device seems to be slightly temperature-dependent as well. The shape of the I-V curve in forward bias does not appear to change much between temperatures except for a decrease in overall current magnitude with decreasing temperature. The shape of the I-V curve in reverse bias does change, however. At room temperature the device is extremely polar, with the leakage current increasing significantly with small increases in reverse bias. When the device is cooled to 100K this polar behavior almost completely disappears.

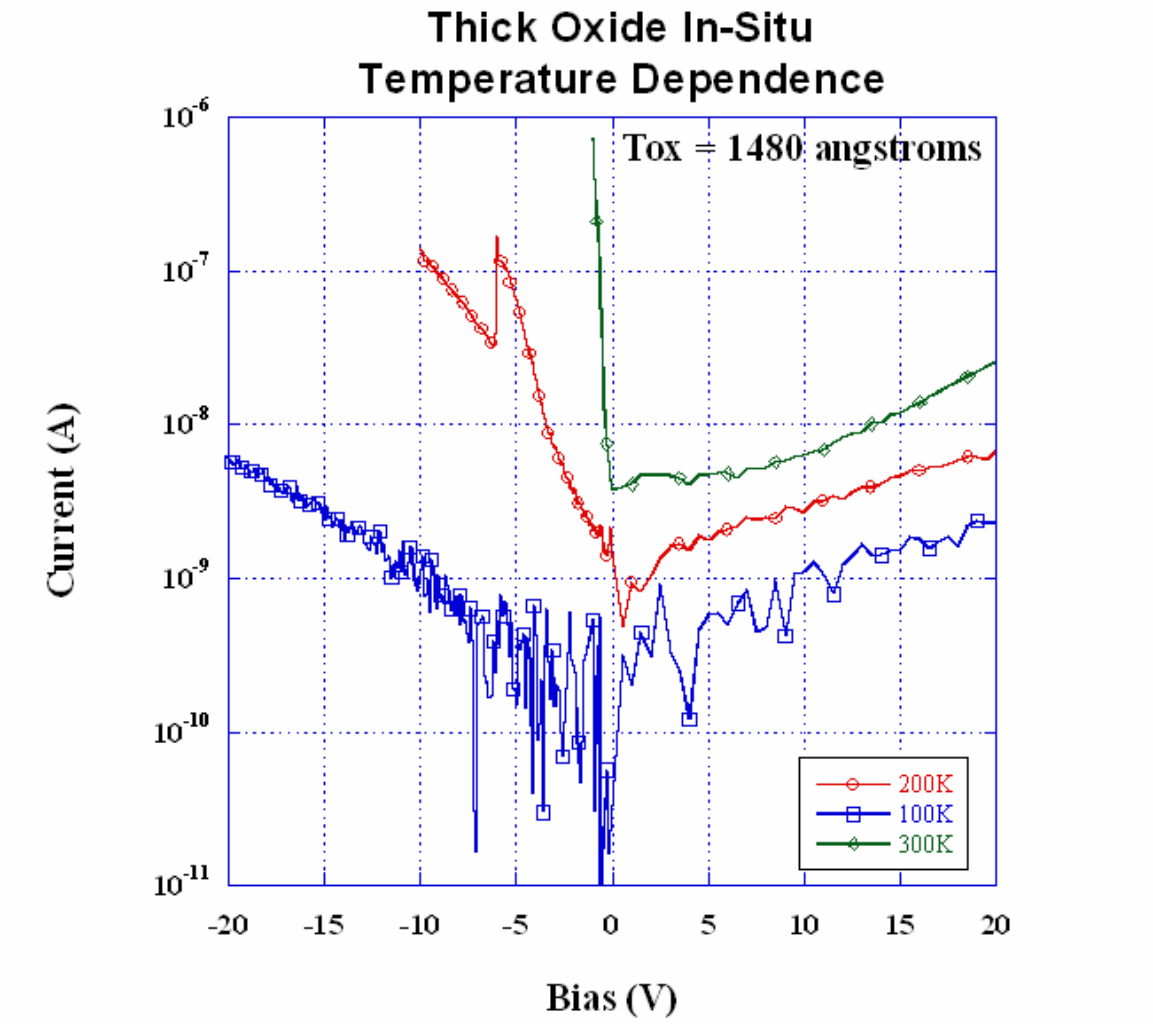

Fig 6.17 Temperature dependence of the current in a thick oxide In-Situ device.

In Fig 6.18 we show the temperature dependence of the thick oxide Pre-Poly device. Much like the In-Situ device, the largest changes with temperature are observed in the reverse bias ranges. The working voltage range in reverse bias increases to approximately -10V at 200K and -20V at 100K much like in the In-Situ device. The biggest differences between the two device types are that the Pre-Poly device is less temperature-dependent in forward bias, and has much lower current levels than the In-

Situ device at both forward and reverse bias. In the low field forward bias range in Fig 6.18, there is a slight decrease in current with temperature. However, as the bias reaches the high field range there is almost no difference between temperatures. Another difference between the two is that the leakage current across the board is slightly less in Pre-Poly than In-Situ. While there are subtle differences in the way each type of device is affected by temperature, they generally exhibit the same trends. At room temperature each type of device has the full working voltage range in forward bias and very little range in reverse bias. When the devices are cooled down to 100K, the polar behavior of these devices is effectively eliminated. The working voltage range in reverse bias is extended out to -20V with leakage current levels comparable to forward bias. The working voltage range in forward bias is fully retained.

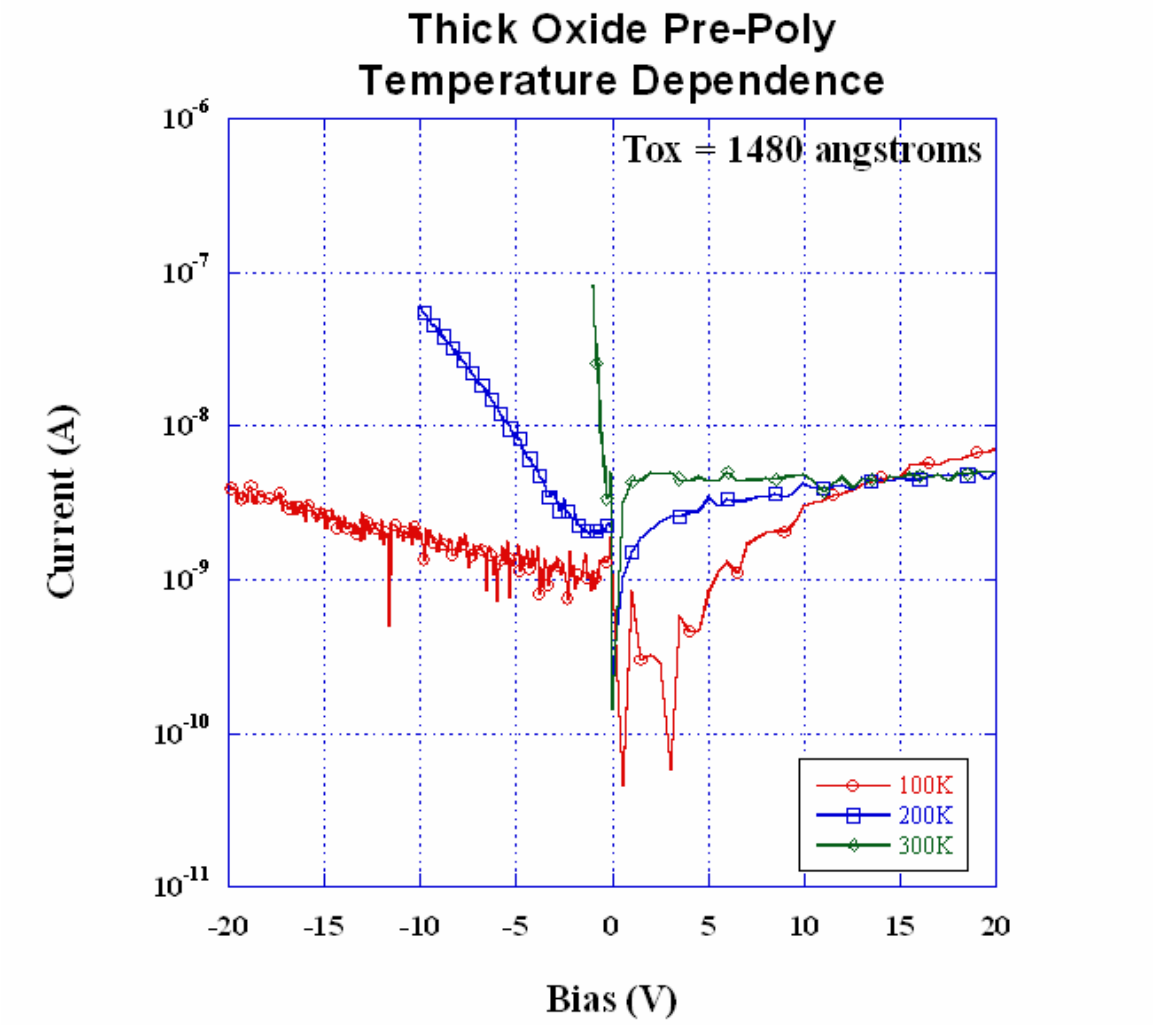

Fig 6.18 Temperature dependence of the current in a thick oxide Pre-Poly device.

6.5.3 Leakage Mechanisms

As previously discussed, using a 65s delay between data points in an I-V measurement will not yield a pure dc conduction current for these devices. However, due to the length of time needed to reach steady-state, as well as the effects the extended stress has on these devices, using the much shorter delay time is our best option for trying to identify leakage mechanisms. After a delay of 65s, the amount of transient current

remaining will be very small compared to the dc leakage current. Therefore, the leakage current should dominate the I-V measurements, allowing us to make qualitative observations about the conduction mechanisms. Since some of the current in each measurement will be due to transient effects, there will be an inherent error associated with each data point. Although small, this error will ultimately prevent us from extracting any accurate quantitative device parameters.

The I-V data discussed thus far has included both forward and reverse bias operation over a range of temperatures. Now we will use I-V data to model the leakage current mechanisms under normal operating conditions. More specifically, the measurements will be made in forward bias at room temperature using the 65s delay in order to obtain a relatively high resolution curve.

First we examined a thick oxide (1480 angstroms) In-Situ device. In Fig 6.19 we show an I-V measurement performed on the device from 0V to approximately 14V. The voltage range was limited in this particular case due to measurement error past 14V. Other than the limited range, the I-V curve appears as would be expected for an MIS capacitor. From the review of conduction mechanisms in Chapter 5, we know that I-V data can be examined on several different characteristic plots. By looking at the data on a semi-log plot, we can search for any regions that suggest particular types of conduction mechanisms.

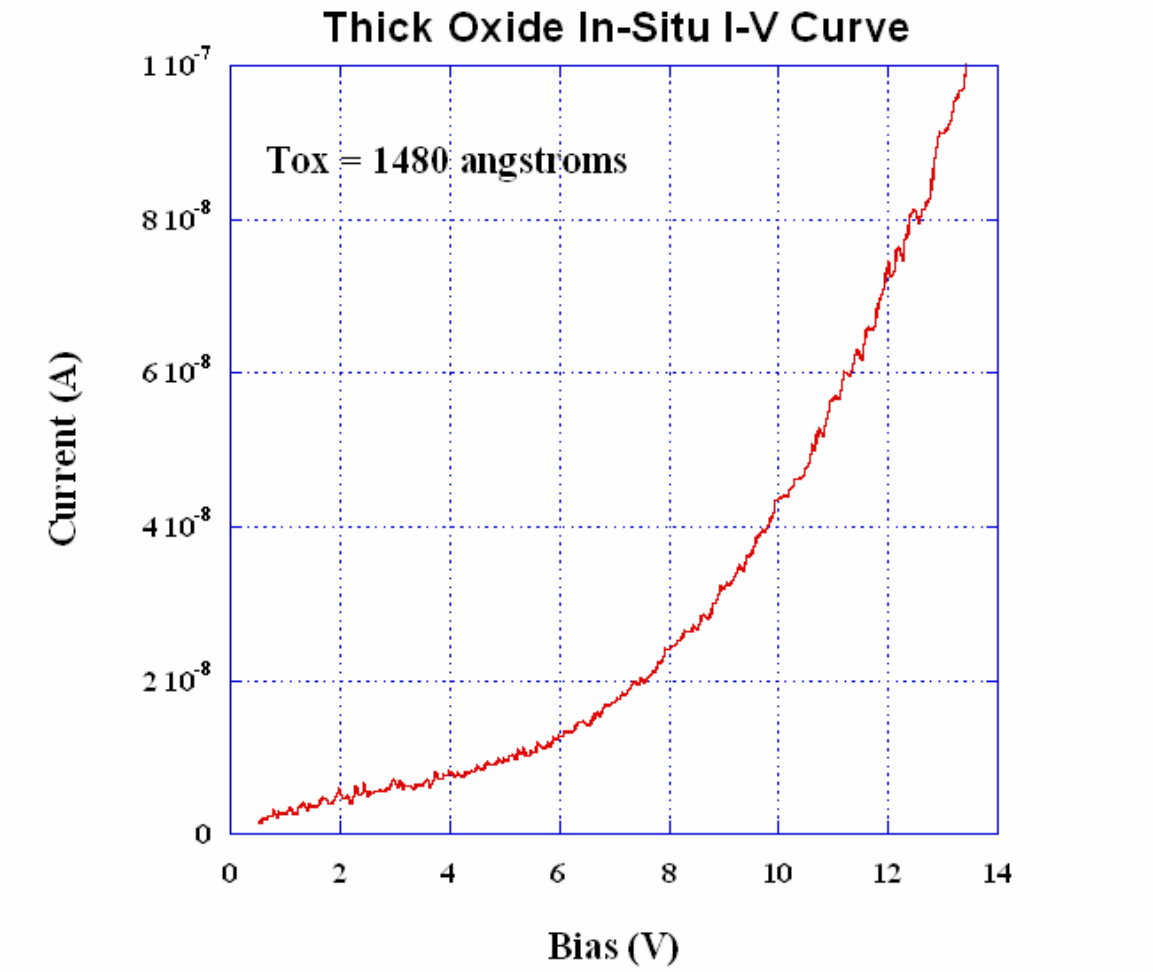

Fig 6.19 Thick oxide In-Situ I-V curve.

In Fig 6.20 we show the data from Fig 6.19 over a voltage range that has a very linear response on a semi-log plot. A linear region on a semi-log plot means that the current varies exponentially with voltage. As can be seen in the curve fit equation in Fig 6.20, this particular range of data from 6V to ~11.5V has an excellent correlation coefficient (R=0.9987) for an exponential curve. Several of the mechanisms from Chapter 5 have an exponential current-voltage relationship such as the Poole-Frenkel Effect, Fowler-Nordheim Tunneling, and the Schottky Effect. We also know from the

literature [31] that the Poole-Frenkel Effect has been observed in modern tantalum capacitors.

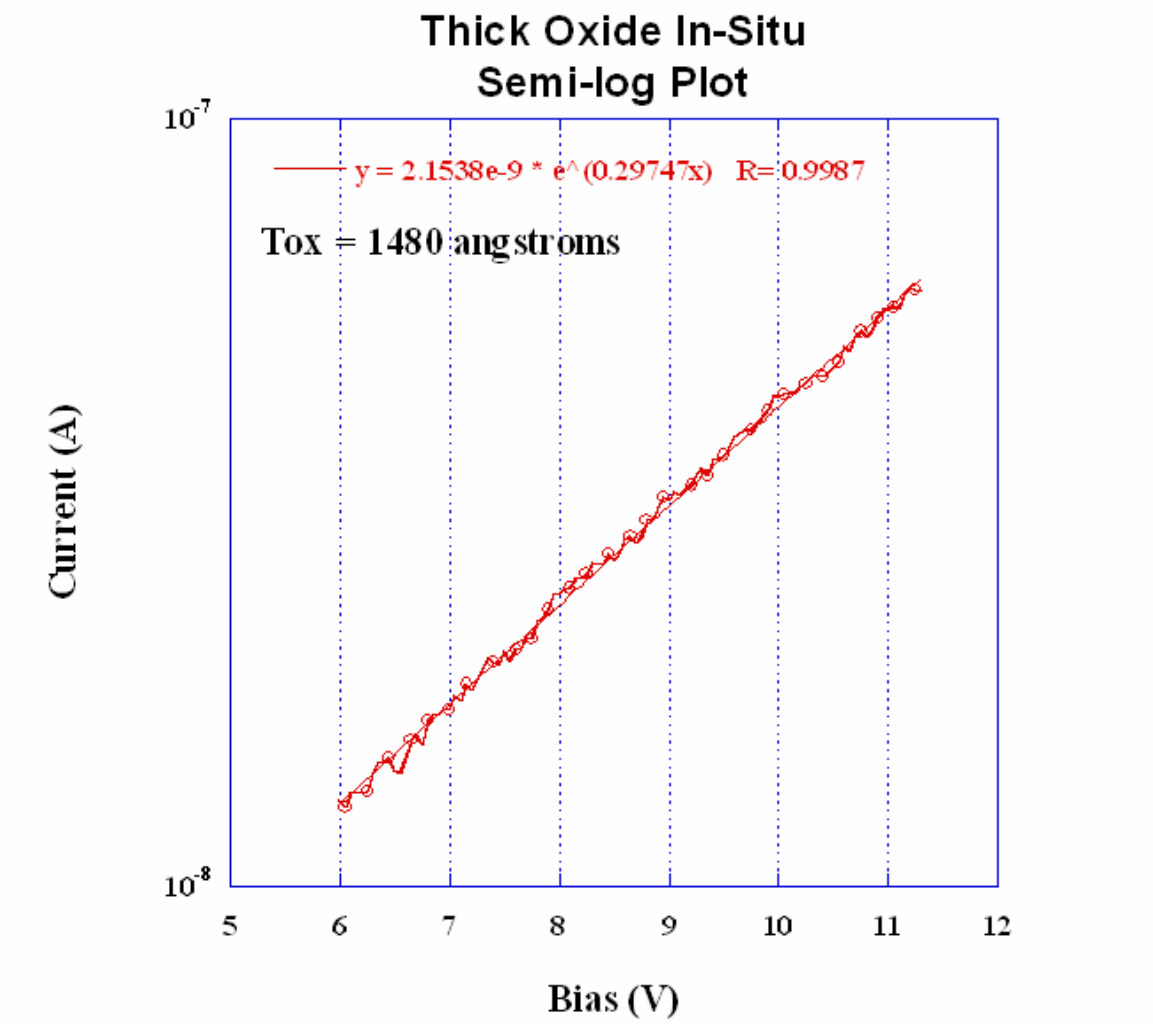

Fig 6.20 Thick oxide In-Situ linear region of Semi-log plot.

In Fig 6.21 we graph the data on a Poole-Frenkel plot. Recall that according to the Poole-Frenkel model, any linear region on a plot of $\ln(J/E)$ versus $\sqrt{E}$ is evidence of PF emission. We plotted the current (I) instead of the current density (J) in this case and we calculated the electric field (E) by taking the applied bias across the associated oxide

thickness. Fig 6.21 exhibits an extremely good linear region on a PF plot. This result yields good evidence that, within the voltage range of 6V to ~11.5V, the Poole-Frenkel mechanism is a dominant contributor to the overall current.

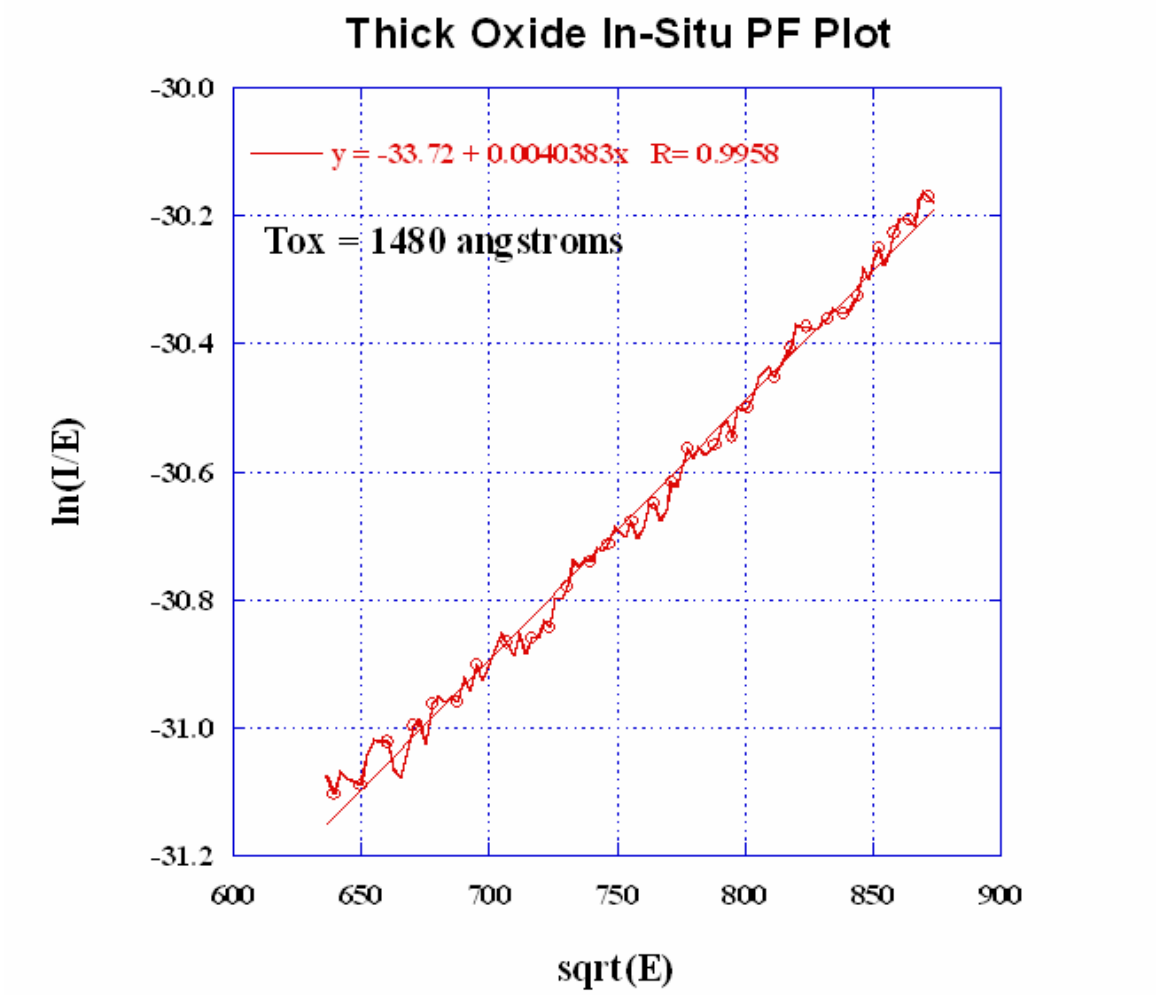

Fig 6.21 Thick oxide In-Situ Poole-Frenkel plot.

Since the data within the voltage range from 6V to ~11.5V is linear on a semi-log plot it is also reasonable to investigate the data for the Schottky Effect. In Fig 6.22 we graph the same data on a Schottky plot. Evidence of Thermionic Emission, the Schottky Effect, will be shown on a plot of $\ln(J_S)$ versus $\sqrt{E}$ as a straight line. Much like the PF

plot in Fig 6.21, the data displays an extremely good linear region on a Schottky plot. The correlation coefficient is also slightly better than that of the PF plot.

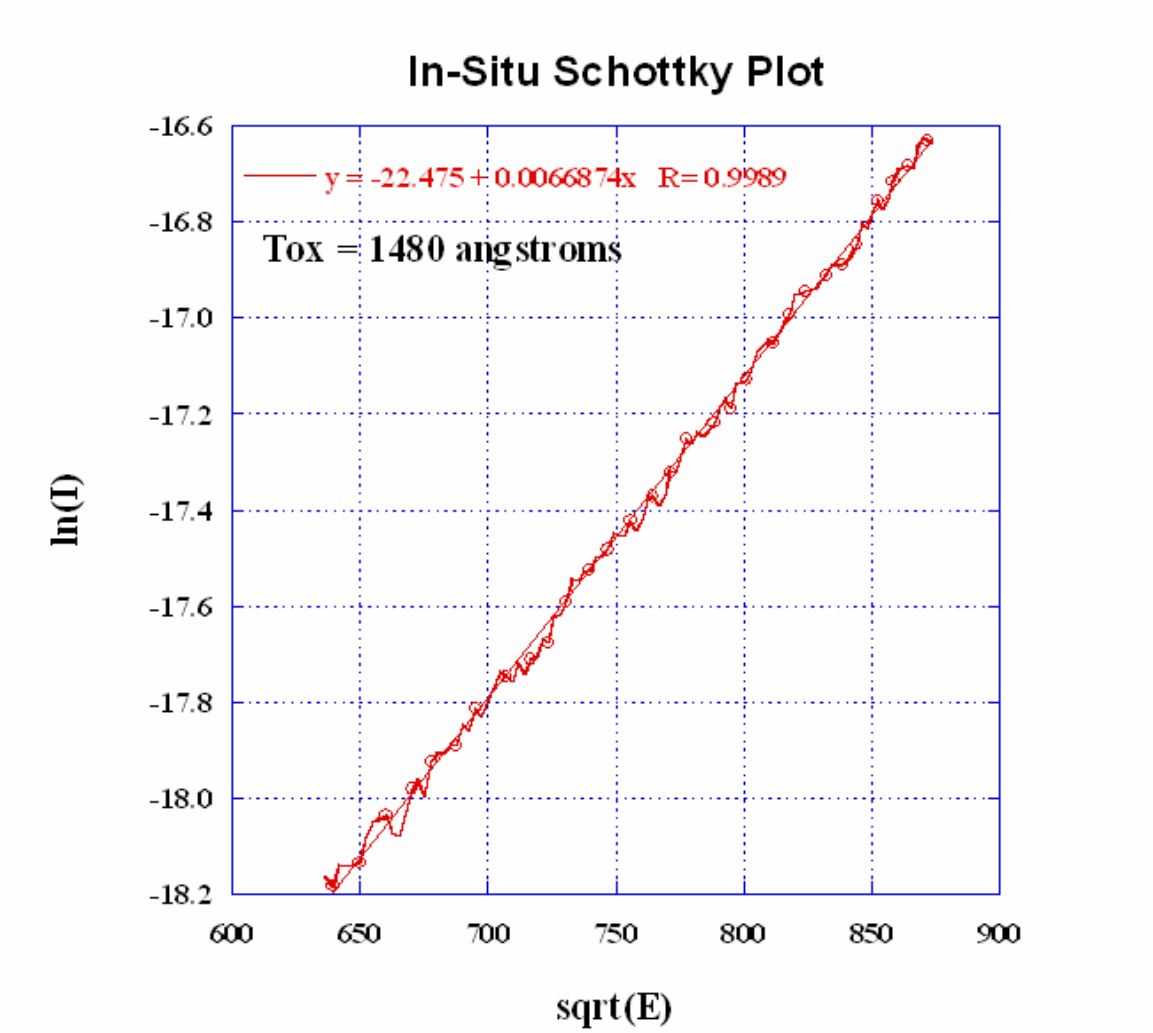

Fig 6.22 Thick oxide In-Situ Schottky plot.

Another characteristic plot that yielded interesting results for the thick oxide In-Situ device was a log-log plot. As can be seen in Fig 6.23, the I-V data displays two distinct linear regions on a Power Law plot. The first region is related to current injection into the oxide with a trap-filled limit [31]. The second region is due to SCLC with a

distribution corresponding to one of the models found in Table 5.1. The second region also overlaps the voltage range in which PF and the Schottky Effect were previously observed. Therefore, the leakage current within this range can be attributed to multiple competing conduction mechanisms.

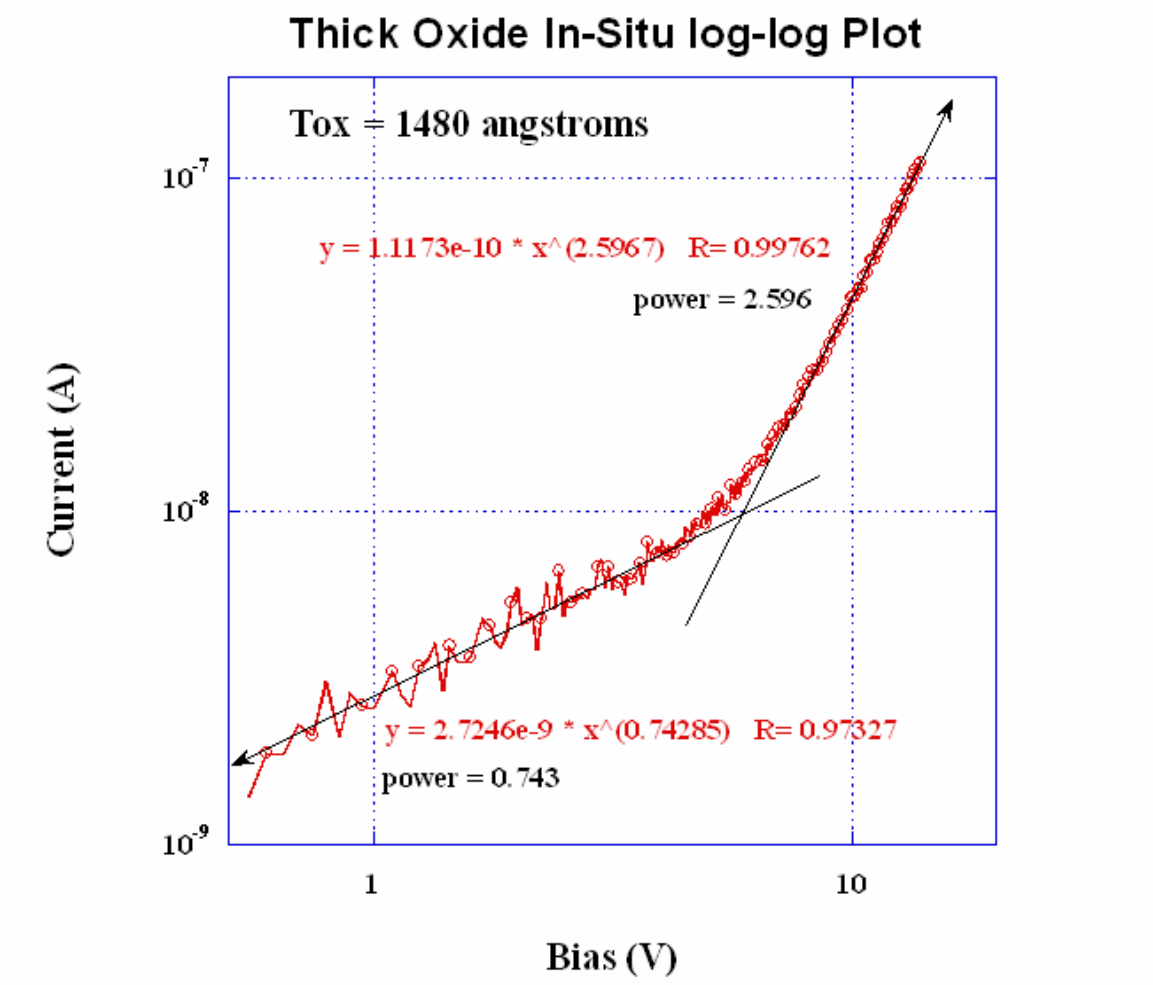

Fig 6.23 Thick oxide In-Situ log-log plot.

Next we will examine a thin oxide In-Situ device. As with the thick oxide In-Situ device, we performed an I-V measurement from 0V to the device's maximum working voltage. In Fig 6.24 we show the I-V data on a semi-log plot. A significant linear region

exists on this plot from 1V to 2.5V, which is evidence that one of the conduction mechanisms with an exponential current-voltage relationship is present.

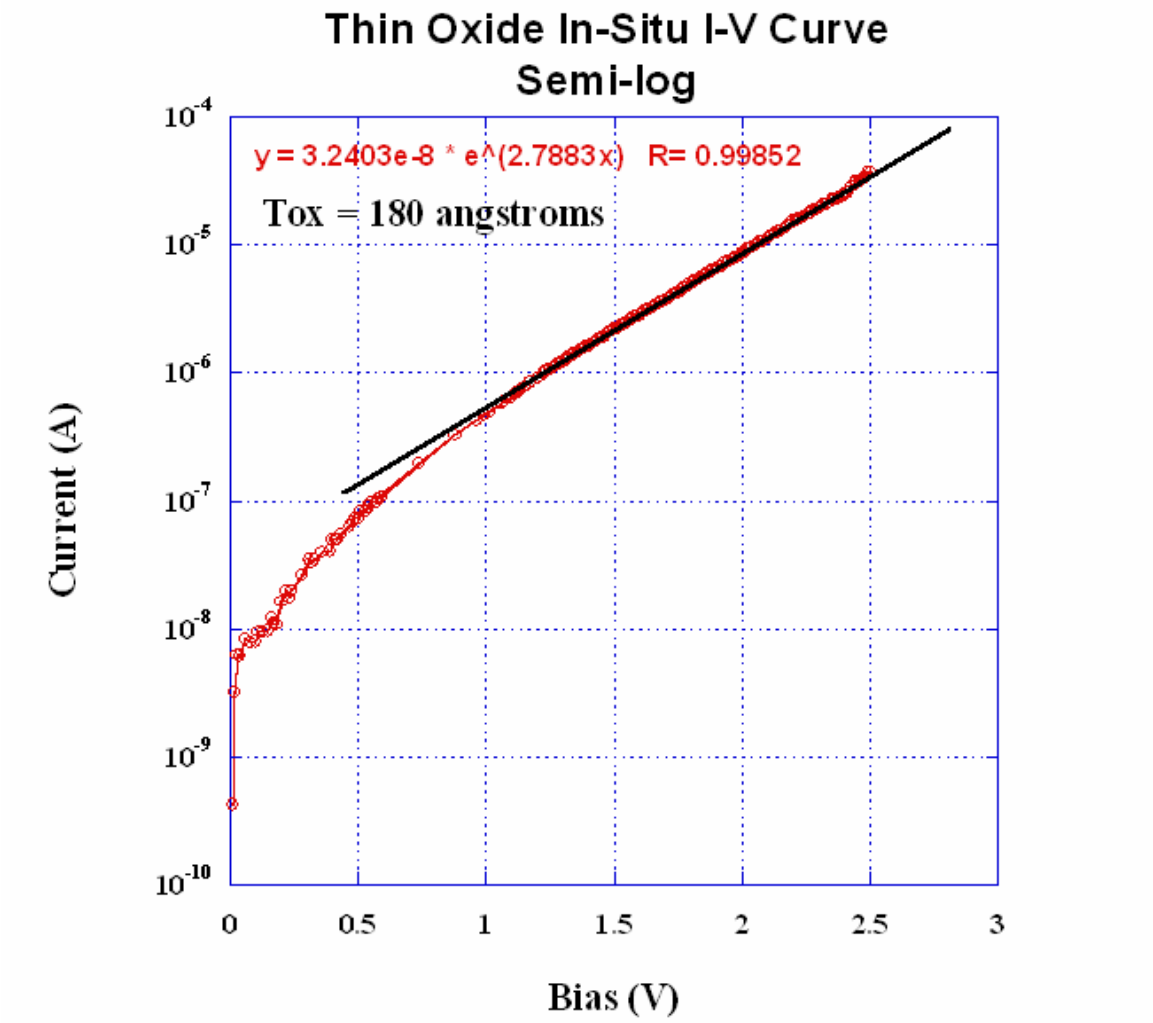

Fig 6.24 Thin oxide In-Situ Semi-log plot.

The data from this linear region was then plotted on a PF plot and is shown in Fig 6.25. This voltage range also exhibits a very good linear region on the PF plot. Much like the thick oxide In-Situ device, the current over a large portion of the working voltage range has significant evidence of Poole-Frenkel emission.

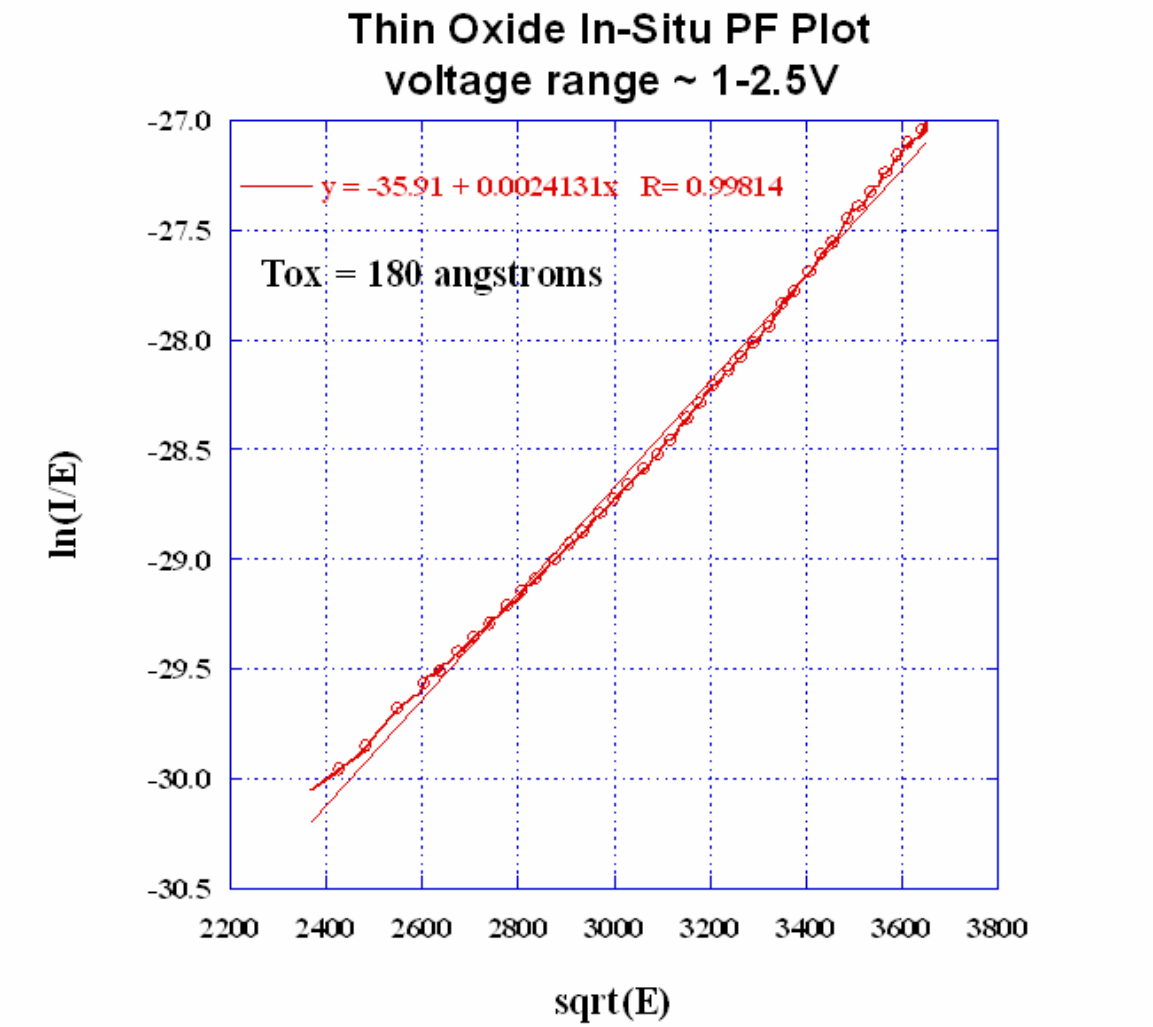

Fig 6.25 Thin oxide In-Situ Poole-Frenkel plot.

We then looked at the same range of data on a Schottky plot, shown in Fig 6.26. In similar fashion to the thick oxide In-Situ device, this data range also exhibited an excellent linear correlation to a Schottky plot. A significant range of the working voltage for the thin oxide In-Situ device displayed strong evidence for the Schottky Effect and PF.

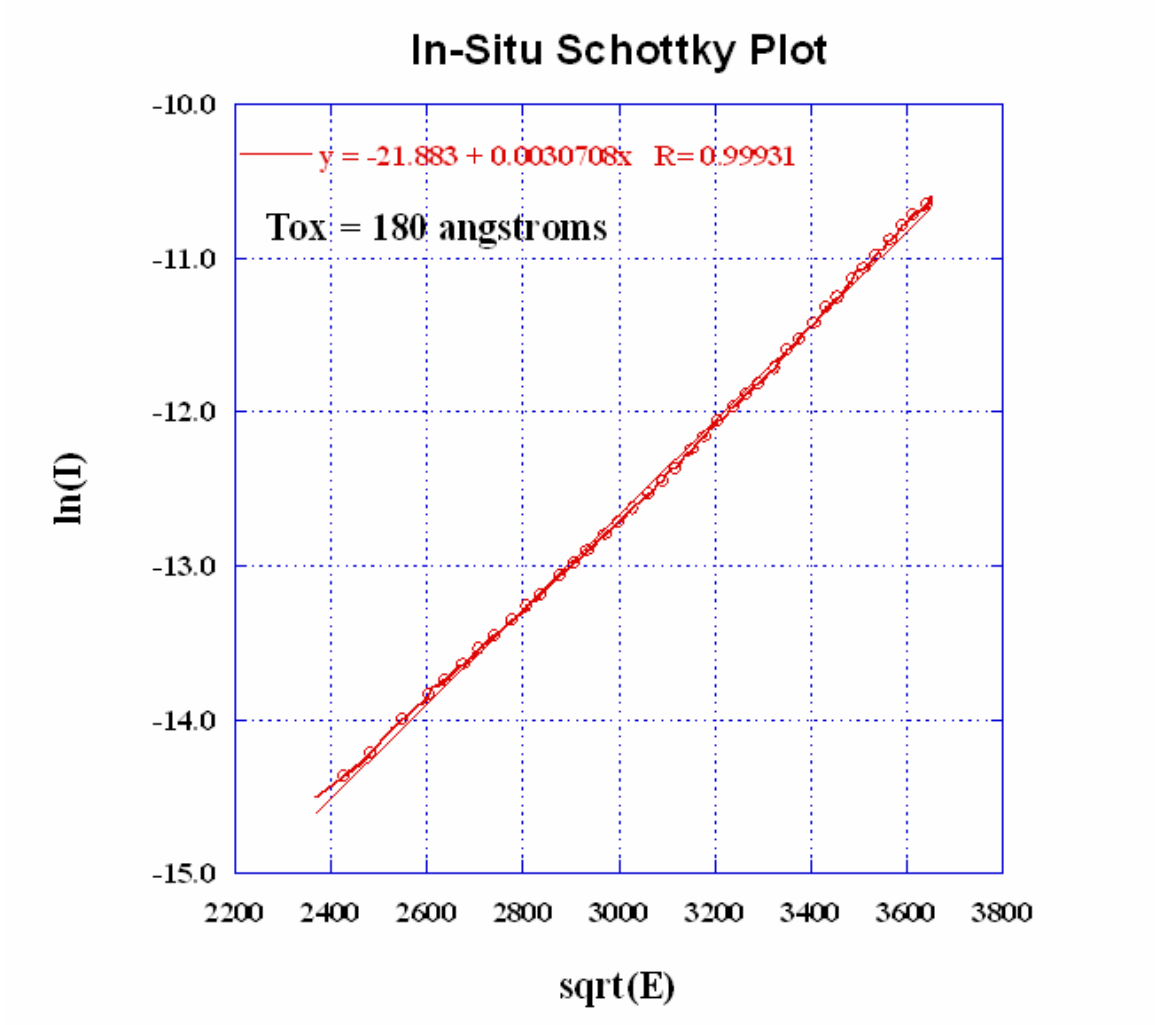

Fig 6.26 Thin oxide In-Situ Schottky plot.

In Fig 6.27 we show the data on a log-log plot, and, similar to the thick oxide In-Situ device, there are two regions of linearity. The power relationships associated with each are much higher than in Fig 6.23 and not much different from each other, so it is possible that both regions are a result of SCLC. None of the other characteristic plots revealed any interesting results for the thin In-Situ device.

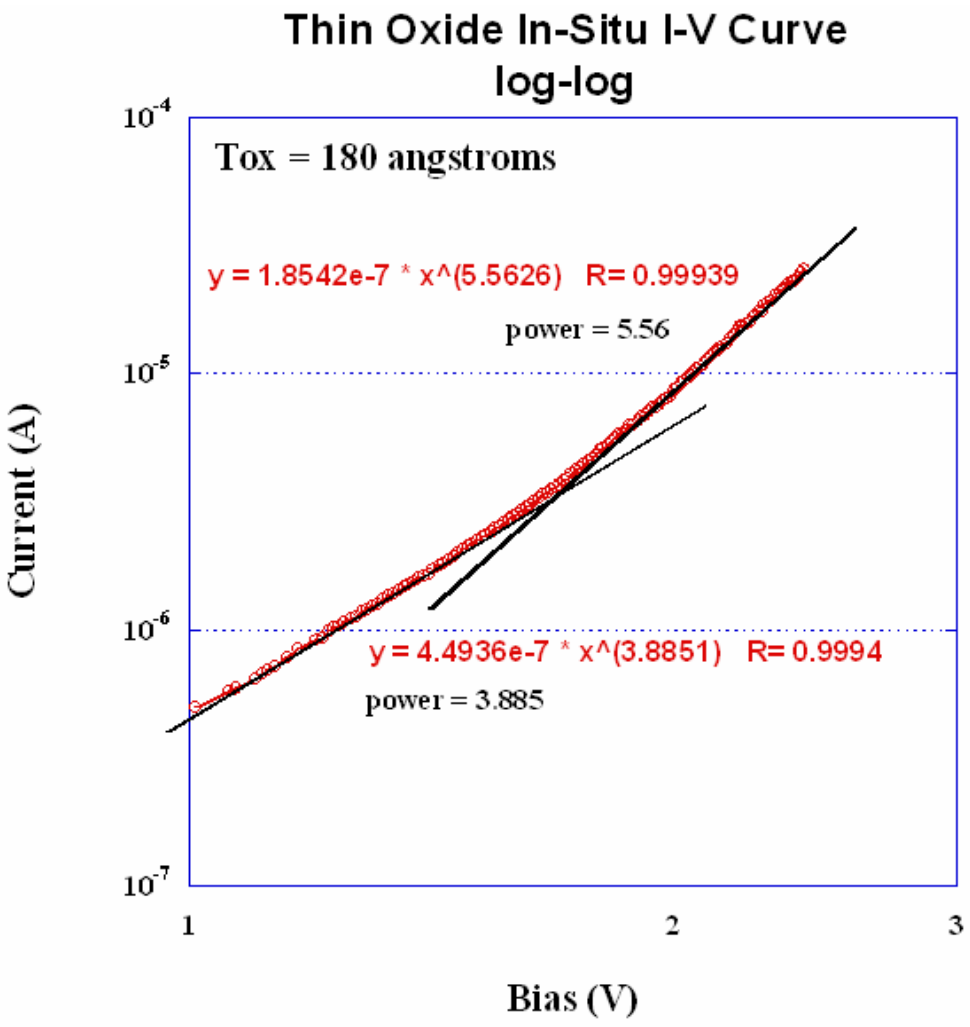

Fig 6.27 Thin oxide In-Situ log-log plot.

Data for the thick oxide Pre-Poly device was collected in a fashion similar to the previous devices. In Fig 6.28 we show the I-V data over the complete working voltage range on a semi-log plot. The current in this device remains relatively constant when compared to its In-Situ counterpart and does not significantly increase until well into the upper voltage range. There are two possible linear regions on this plot, suggesting that

one conduction mechanism is dominant transitioning into a separate mechanism around 15V.

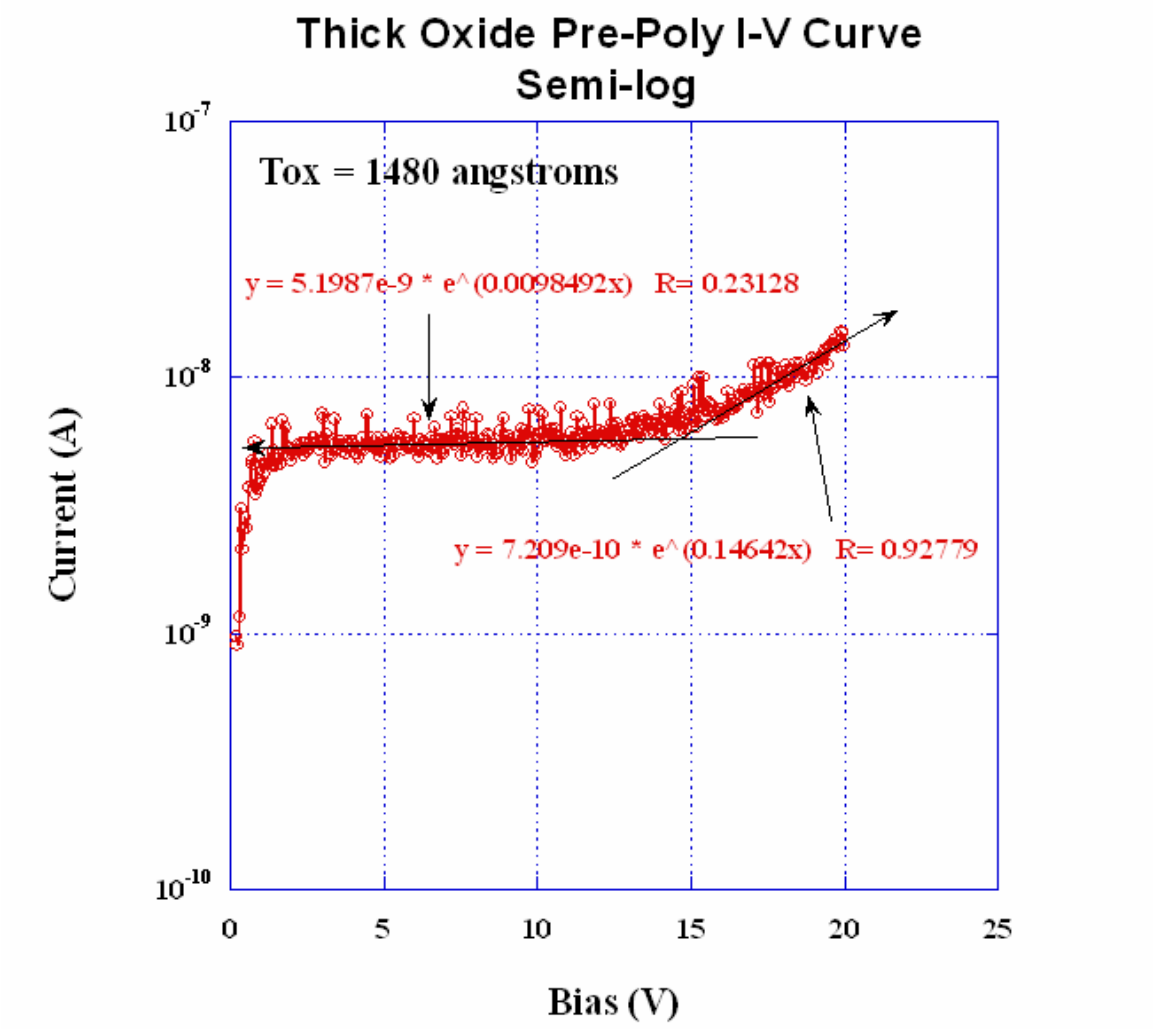

Fig 6.28 Thick oxide Pre-Poly Semi-log plot.

We first looked more closely at the low voltage linear region. After plotting this data on various characteristic plots, we found a relatively good correlation to Fowler-Nordheim Tunneling. In Fig 6.29 we show a FN plot with a linear region existing from approximately 7.5V to 16V.

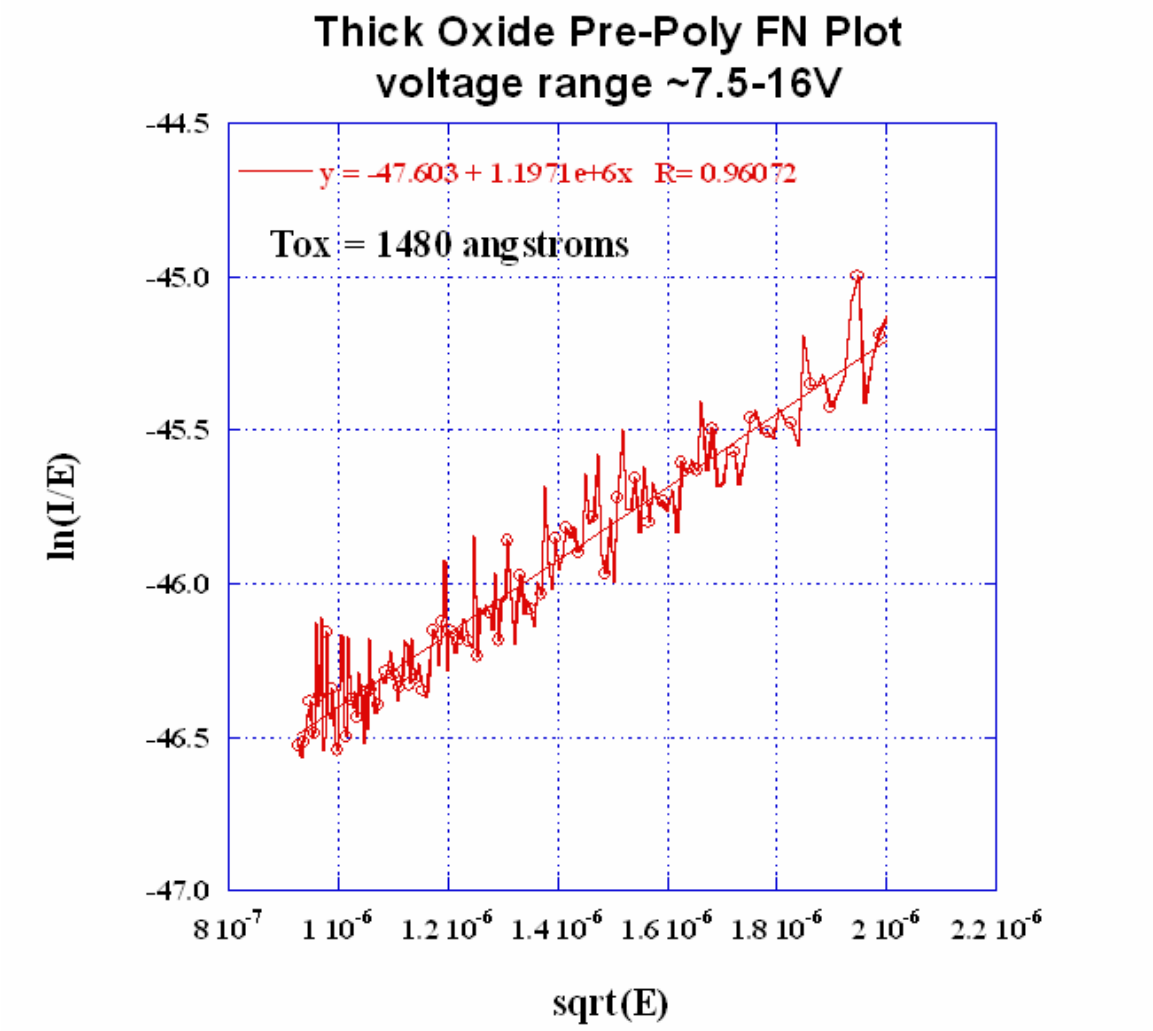

Fig 6.29 Thick oxide Pre-Poly Fowler-Nordheim plot.

The linear correlation on the FN plot is reasonable for this range of data but shows quite a bit of variation. When examining this plot in the context of the semi-log plot in Fig 6.28, FN Tunneling appears to be present but is also a relatively weak mechanism as the current is fairly constant.

Next we looked at the high-voltage linear region, from ~16V to 20V, in Fig 6.28 which correlated somewhat to both PF and Schottky plots. In Fig 6.30 we show a PF Plot

for the voltage range from 16V-20V. The data does not display a very good linear region according to the fit equation. However, even though the data shows quite a bit of variation, there is a definite linear trend associated with it.

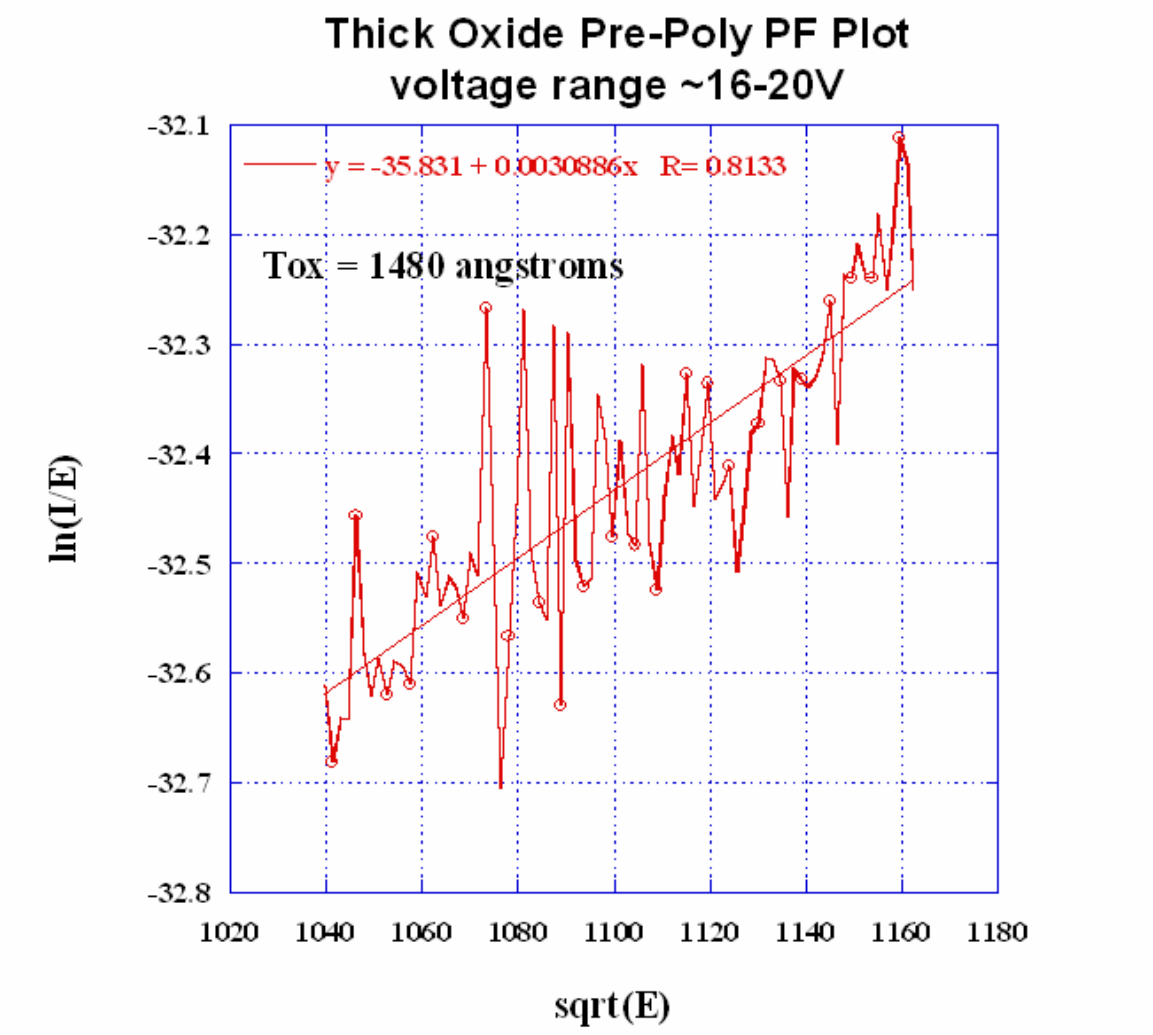

Fig 6.30 Thick oxide Pre-Poly Poole-Frenkel plot.

In Fig 6.31 we show the same data between 16V-20V on a Schottky plot. The data shows a slightly better linear region according to the fit equation, and definitely

appears to show a linear trend. However, the data still shows a large amount of variation and does not appear to follow the model very well.

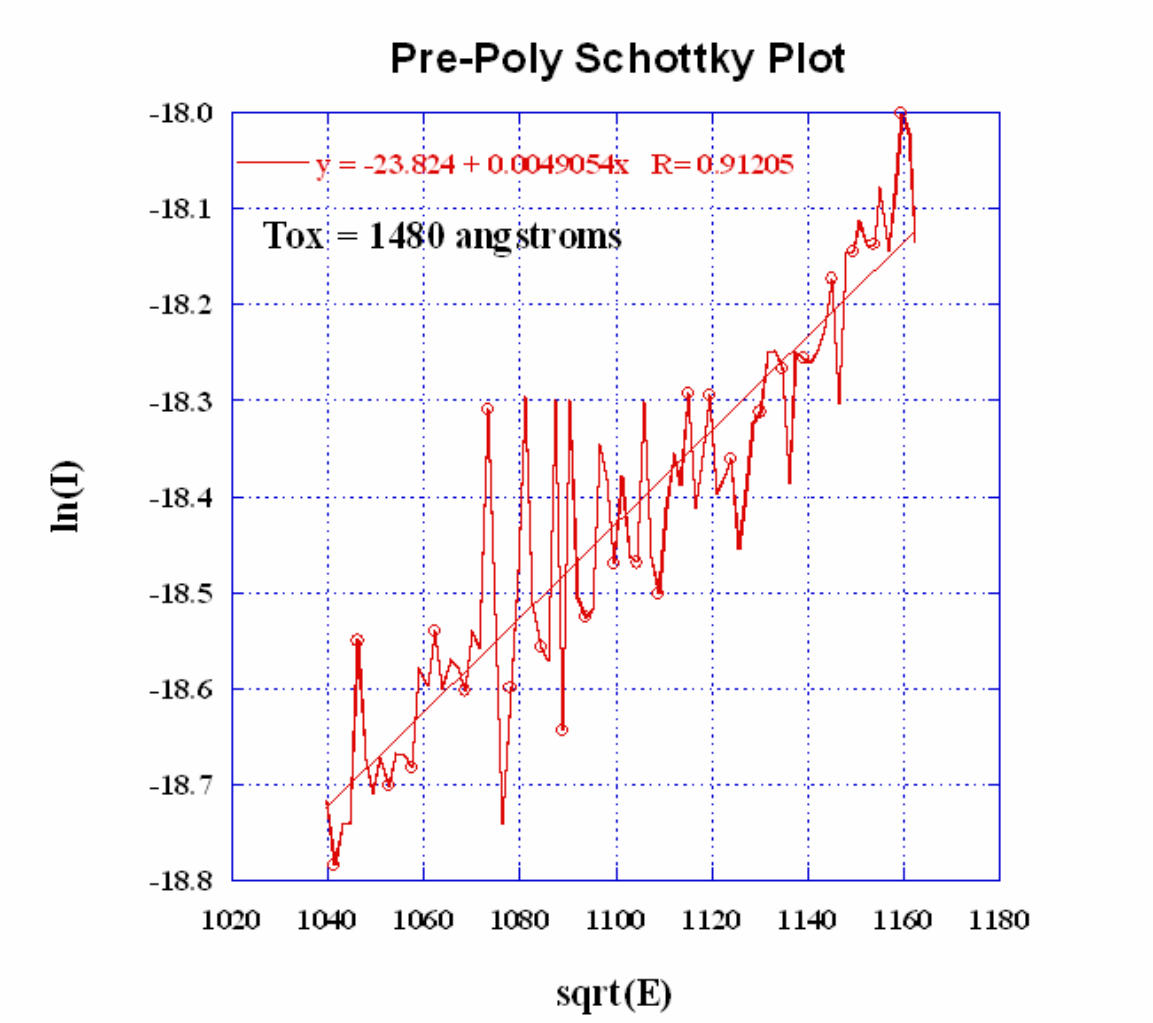

Fig 6.31 Thick oxide Pre-Poly Schottky plot.

The I-V data for a thin Pre-Poly device is shown in Fig 6.32 on a semi-log plot. A linear region is observed between ~1V and 2.5V. We found that the linear region correlated very well to a PF plot. In Fig 6.33 we show the PF plot for this data. Unlike

the thick oxide Pre-Poly device, this particular device did not show any evidence of FN Tunneling.

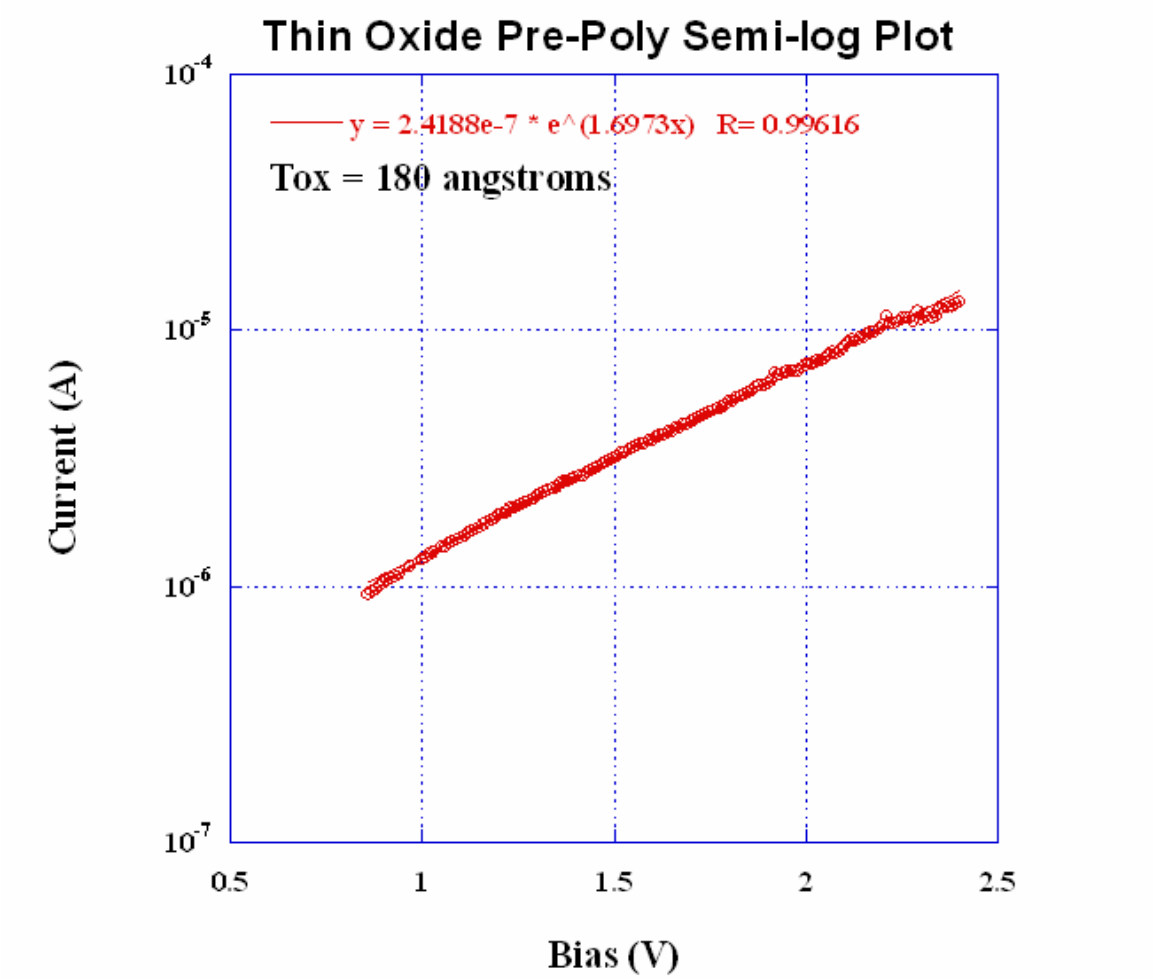

Fig 6.32 Thin oxide Pre-Poly Semi-log plot.

This range of data was also plotted on a Schottky plot. In Fig 6.34 we show a very good correlation to a linear region on the Schottky plot. Based on both visual observation and the correlation coefficient to a linear fit, the data fits the Schottky model much more strongly than the PF model.

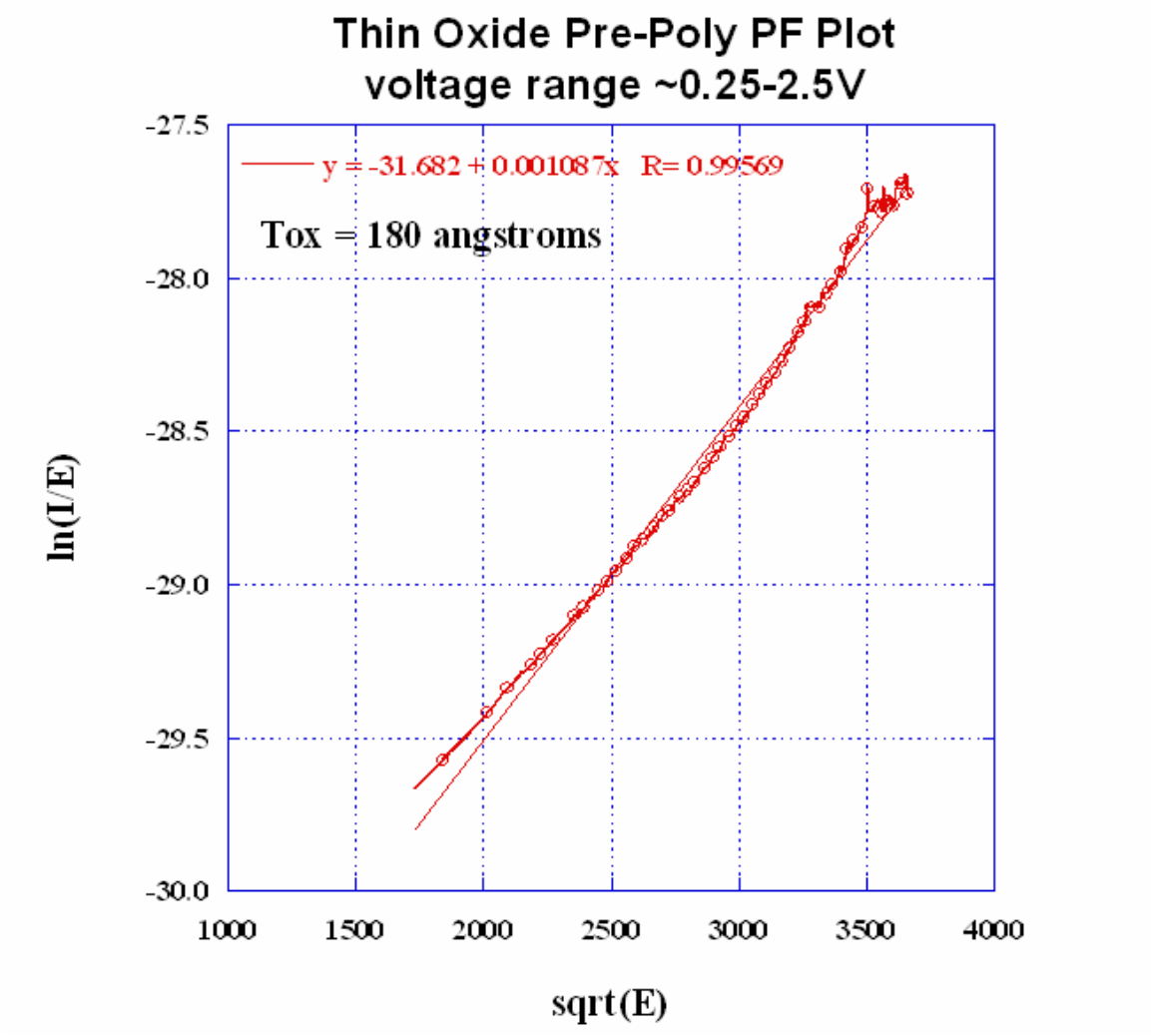

Fig 6.33 Thin oxide Pre-Poly Poole-Frenkel plot.

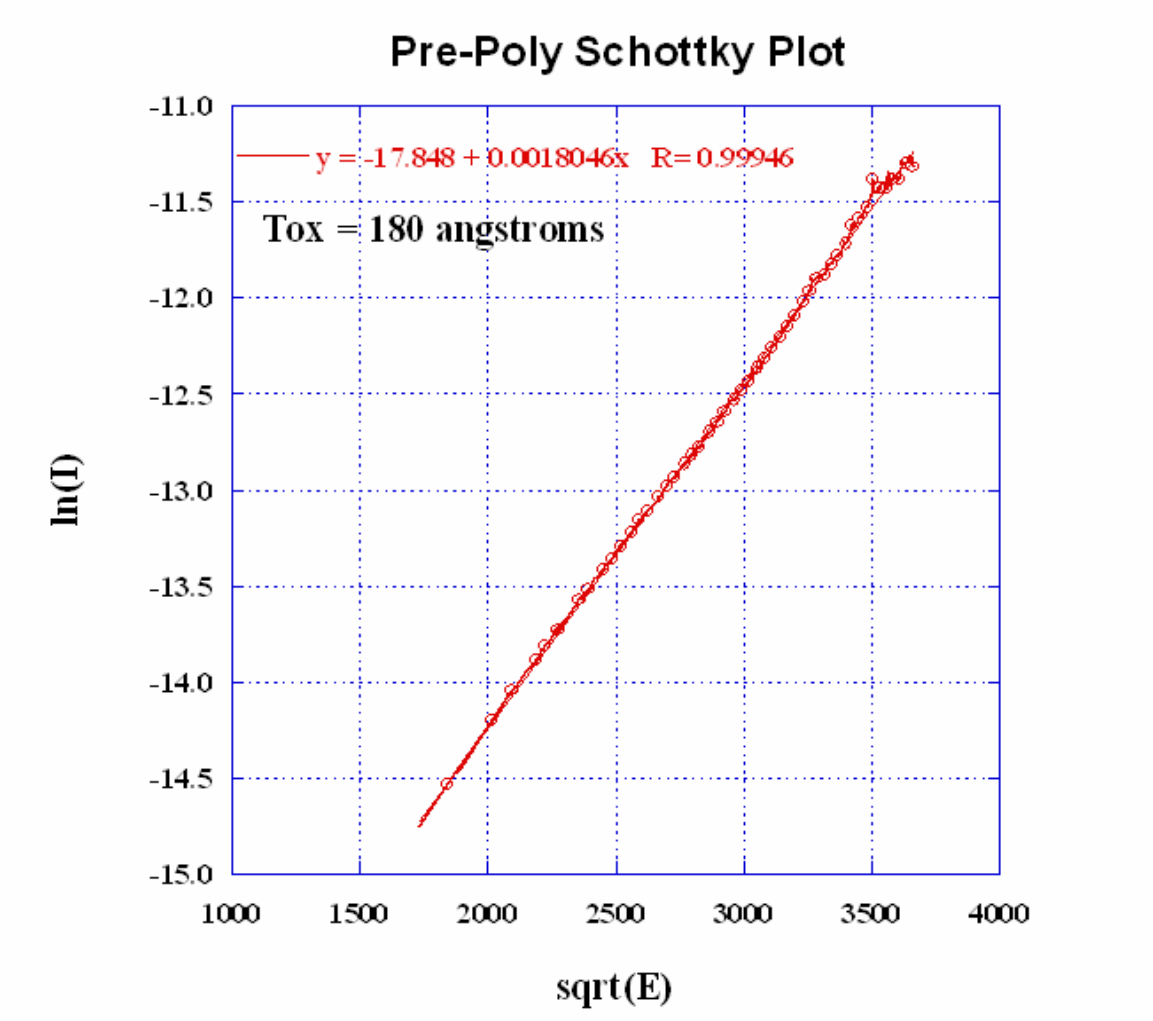

Fig 6.34 Thin oxide Pre-Poly Schottky plot.

The devices of each type and oxide thickness that were investigated showed evidence of several specific conduction mechanisms. Both In-Situ devices revealed a combination of the Poole-Frenkel Effect, the Schottky Effect, and SCLC. While the thick oxide Pre-Poly device showed a combination of the Poole-Frenkel Effect, the Schottky Effect, and Fowler-Nordheim Tunneling, the thin oxide Pre-Poly device showed only the Poole-Frenkel Effect and the Schottky Effect. The fact that these mechanisms are

observable on characteristic plots is significant evidence to suggest that they exist within these devices. However, we cannot say that these mechanisms are solely responsible for all the current. Each measurement still has a certain amount of transient current as well as possible current components due to other conduction mechanisms not considered in this thesis.

6.6 Conclusion

In this chapter we made characteristic measurements on modern tantalum capacitors in a fairly radical manner. The basis for these measurements was the assumption that modern tantalum capacitors have materials similar to traditional MIS devices and therefore perform similarly as well. Due to the different materials and complex geometry of the tantalum capacitors, we made modifications to C-V, I-V, and I-t measurement parameters in order to suit our needs for these devices. Through C-V measurements we were able to observe voltage-dependent capacitances that showed similarities to MIS theory. By making these measurements at various temperatures we were also able to determine that the capacitance of these devices is very temperature-dependent. I-t measurements were used to estimate the amount of time necessary for the transient response to settle at specific biases. Due to the extended stress placed on the devices by sequential I-t measurements, I-V measurements were made using much smaller delay times than those needed to reach steady-state. Although this decision introduced a small amount of error into each measurement, we were still able to observe conduction mechanisms on several characteristic plots. In-Situ devices produced regions of leakage current that could be attributed to the Poole-Frenkel Effect, the Schottky

Effect, and Space-Charge-Limited Current, while the Pre-Poly devices showed evidence of the Poole-Frenkel Effect, the Schottky Effect, and Fowler-Nordheim Tunneling. These measurements confirm our overall assumption that modern tantalum capacitors can be electrically characterized in a manner similar to MIS devices.

The In-Situ and Pre-Poly devices are nearly identical in terms of device structure. Essentially the only difference between the two is how the PEDOT layer is deposited and polymerized during the manufacturing process. The nominal zero bias capacitance of each type is fairly similar, but when the performance characteristics are investigated more closely there are many differences between them. The room temperature capacitance at all bias levels was much more consistent between samples in the Pre-Poly devices than the In-Situ devices. The capacitance of the Pre-Poly devices also tended to be tens of microfarads lower. When investigated as a function of temperature, the Pre-Poly capacitance was found to be extremely temperature dependent where as the In-Situ capacitance was not nearly as much so. The current characteristics of each type of device also tended to differ. As previously mentioned there was evidence of different leakage current conduction mechanisms found in each type of device. While leakage current was definitely observed in all devices, the current in In-Situ devices tended to increase more significantly with an increase in bias than it did in Pre-Poly devices.

The possible reasons for these differences lie in the PEDOT polymer layer. According to KEMET, In-Situ polymerized PEDOT tends to be composed of small molecules that penetrate defect sites in the dielectric [48]. In doing so the polymer layer more completely covers the dielectric layer, allowing less moisture to be trapped, which

would, in turn, cause the capacitance to be less temperature dependent. However, by penetrating the defect sites In-Situ polymerization also interferes with the dielectric layer thus reducing the breakdown and working voltages and causing poorer electrical characteristics. On the other hand, Pre-Polymerized PEDOT is composed of larger molecules that remain on the surface and allow more trapped moisture, but do not interfere with the dielectric layer giving Pre-Poly devices more temperature dependence and better electrical performance [48]. By cooling the devices to 100K we were able to show that the capacitance was reduced by an amount equal to or greater than it was by drying the devices, which was done by KEMET in a separate test. This reduction was much greater for the Pre-Poly devices than for the In-Situ devices. This result supports the model the Pre-Poly PEDOT leaves larger moisture-filled gaps in the polymer coverage, than does the In-Situ PEDOT.

CHAPTER SEVEN

SUMMARY AND CONCLUSIONS

In this research, the electrical characterization of modern tantalum capacitors manufactured by KEMET Electronics Corporation was presented. The two main classifications of devices that were investigated were In-Situ and Pre-Poly devices. Within these classifications there were also several levels of working voltages, or oxide thicknesses. The terms In-Situ and Pre-Poly refer to the manner in which the PEDOT was polymerized and applied during manufacturing of the devices.

The main goals in characterizing these devices were to observe behaviors predicted by MIS theory on characteristic C-V plots, identify mechanisms of leakage current conduction, and compare the differences between In-Situ and Pre-Poly devices. In order to accomplish these goals, the characteristic measurements that were made included C-V measurements, I-t measurements, and I-V measurements. In addition, some of these types of measurements were investigated as a function of temperature. Due to large amounts of leakage current in reverse bias operation, the C-V measurements were initially conducted at low temperatures (100K). Through these measurements we were able to observe voltage-dependent capacitance data that showed some similarities to the theoretical MIS modes of operation. Measurements at 300K also showed signs of voltage dependencies; however, in both cases the range of operation of the devices proved to be too limited to observe a complete C-V curve. It is possible that the electric field needed to observe a complete C-V curve is so high that the device would fail before it could ever be reached.

By comparing measurements at 100K to those at 300K we were able to observe some interesting temperature dependencies in these devices. As the devices were cooled, the capacitance of each dropped significantly. This capacitance "loss" occurred much more so in the Pre-Poly devices. The effect temperature had on these devices was largely related to excess moisture that was theorized by KEMET to be present in the polymer layer due to incomplete coverage of the dielectric. By making low temperature measurements, we converted the water (κ=81) to ice (κ=1). This observation corresponded very well to measurements KEMET had performed on devices that had been dried, giving validity to their model that Pre-Poly devices did not have complete polymer layer coverage.

While both In-Situ and Pre-Poly devices were manufactured to have equivalent levels of performance and capacitance, they displayed several differences. The zero bias capacitance of In-Situ devices was tens of microfarads higher on average, as well as much less temperature dependent than the Pre-Poly devices. The electrical performance of the Pre-Poly devices was the better of the two, showing much lower and more consistent levels of leakage current across all bias ranges. These differences are a result of the different polymerization techniques. Pre-Polymerization created bigger PEDOT molecules that remained on the surface of the dielectric and trapped more moisture, thus making them more temperature dependent. In-Situ polymerization created smaller molecules that more completely covered the dielectric surface but also penetrated macro defects and, in turn, interfered with the dielectric layer causing poorer electrical performance.

I-t measurements were used to observe the significant transient effects in the devices. While they were initially intended to be used to create a point-by-point I-V curve, this task proved to be too straining on the devices. Instead I-t measurements were used mainly to justify settings used for I-V measurements. The I-V measurements were made knowing that they inherently included some error due to short delay times between measurements. For this reason we were never able to extract any quantitative data from I-V measurements. However, we were still able to observe and identify evidence of several conduction mechanisms present in the devices. In the In-Situ devices we found evidence of the Poole-Frenkel Effect, the Schottky Effect, and Space-Charge-Limited Current, while in the Pre-Poly devices we found evidence of the Poole-Frenkel Effect, the Schottky Effect, and Fowler-Nordheim Tunneling. These observations are not intended to be definitive conclusions as to the only conduction mechanisms in modern tantalum capacitors.

While the I-V measurements yielded some very strong evidence of several conduction mechanisms, it is still just evidence and not proof of their existence within these devices. The strongest evidence pointed towards Thermionic Emission as a main conduction mechanism. However, because these materials and devices are not nearly as well characterized and understood as traditional semiconductor-based MIS devices, we cannot with any great degree of certainty say which mechanisms are and which are not present. According to the methods used in this thesis research, the only way to distinguish between Thermionic Emission from the Schottky Effect and the Poole-Frenkel Effect is by measuring the slope on the characteristic plots of each.

Unfortunately due to the small error inherent in the way in which we conducted our measurements, we can only make qualitative observations about our data.

While only qualitative, our results did display a slightly stronger correlation to the Schottky Effect. Also, we know from KEMET that they believe current conduction to be related to PEDOT/dielectric materials issues giving more credibility to the interface-limited Schottky Effect model [48]. In order to investigate this subject further, future research is already being planned with KEMET using flat sample Ta capacitors that have yet to be manufactured. The hope is that by removing the complicated geometric structure from the equation, quantitative data can then be extracted from characteristic plots. Research on these flat samples should be able to determine exactly which conduction mechanisms are present as a result of the pure materials interactions.

Results based on contributions from this research as well as from data collected by KEMET are currently being compiled for two future publications. “Electrical Characterization of Tantalum Capacitors with Poly(3,4-ethylenedioxythiophene) Counter Electrodes” [48] will be submitted to the Journal of the Electrochemical Society, and "Electrical Characterization of Polymer Tantalum Capacitors” [49] is being submitted to the 2008 Capacitor and Resistor Technology Symposium (CARTS 2008).

APPENDIX

Cooling the Cryostat

1. Fill the Dewar with liquid nitrogen.
2. Place the cryostat head on the Dewar by inserting the siphon tube into the tank.
3. Secure the head to the Dewar by attaching the ring clamp.
4. Verify that the plug vent is open (valve handle is parallel with barbed hose connector).
5. Remove the brass ring and cryostat cap to place the device under test (DUT) on the cold chuck.
6. Connect leads to the device (red cable for positive lead, black for negative lead).
7. Replace the cryostat cap and gently tighten the brass ring.
8. Attach the temperature controller and measurement cables to the cryostat.
9. Connect the rotary pump to the exhaust value with the plastic tubing.
10. Connect the electromagnetic pump to the circulation pump inlet with plastic tubing and the blue Swagelock.
11. Turn on the temperature controller. Verify that the heater is off and sensor is reading ambient temperature.
12. Turn on the roughing pump and slowly open the exhaust value (counter-clockwise) to de-gas the chamber; leave the roughing pump on.
13. Turn on the Variac power supply and set to ~20% to begin cooling.
14. Verify that the system is cooling and leave the power supply at ~20% for at least five minutes.

15. Input the desired temperature set point into the temperature controller and set the heater to high (heater will not turn on until temperature has dropped below the set point).
16. Set the power supply to ~30%. The system will take approximately 20-30 minutes to stabilize and will reach at least 100K at this setting.
17. To bring the system back to room temperature, close the exhaust value before turning off both pumps and the heater. The system will equalize by itself or you can use the heater and set the temperature controller to ambient temperature to speed the process.
18. Always bring the cryostat to room temperature before opening the sample chamber (chamber must be re-pressurized to open).
19. When refilling the Dewar tank, verify that the cryostat siphon stem and internal coils are at room temperature before reinsertion. Trapped moisture can block circulation in the system. Warm with a hair dryer or circulate dry room temperature air through the system to drive out moisture.

Making C-V Measurements with Agilent E4980A Precision LCR Meter

1. Connect the lead cables as shown in Fig A-1.
2. Due to the large capacitance and low resistance of the device, set the measurement mode to Cs (series resistance).
3. Set the frequency to one of the capacitor test frequencies (120Hz or 1kHz).
4. Set the measurement time to long.

5. Press the Measurement Setup key. Set the step delay to the desired time between measurement points (600s for 10min delay).

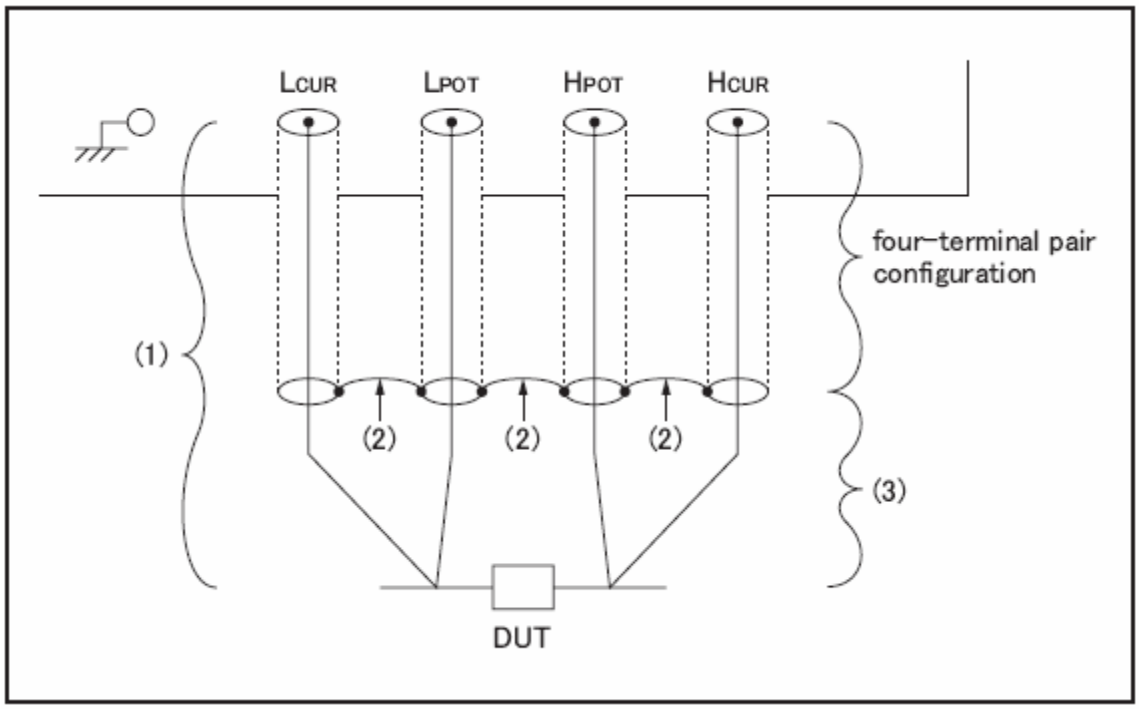

Fig A-1 Lead cable connection diagram.

6. In the Measurement Setup menu, press the list setup softkey. Highlight the list sweep parameter (freq by default) and use the softkey menu on the right to set it to Bias [V]. Enter the bias values to be swept into the list. You can set the first and last point and use the fill linear or fill log options to complete the list.
7. Before any measurement is made a record log must be started. Press the Save/Recall key, then press the Save Data softkey, and then the Start Log softkey to begin the record log.
8. To begin the measurement, press the List Sweep softkey from the main display. This will bring you to the list sweep you just created in Step 6. To start the

measurement, press the DC Bias key. Press the DC Bias key again to stop the list once the measurement is complete.

9. To write this measurement to an Excel file, insert a Flash drive into the USB port on the front of the unit. Press the Save/Recall key, then the Save Data softkey, and finally the Save & Stop softkey. This will write a file to the drive in the USB port. All files will be written to a folder named E4980A and will be sequentially numbered.

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